Exploring Bits Identities of ATPG Sets in Fault Detection and Generating High Quality Patterns to Excite/Observe Targeted Faults

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Abstract

A high quality pattern can be guaranteed to excite or observe a targeted defects without detect the other ones. We investigate each bit's identity of an ATPG set corresponding to a stuck-at hard fault of the circuit, and generate excitation or observation pattern consisting all bits required to excite or observe this hard fault. This high quality pattern is more efficiency-oriented for fault detection than the original ATPG set.

I. Introduction

The ultimate goal of testing is to accurately identify the defective parts. A test set with high quality can be guaranteed to detect the targeted fault.

In order to detect a defect, two requirements must be met. First, the defect must be excited so that the logic value at the location of the defect is different in a defective circuit and a good circuit. Second, the incorrect logic value must be propagated to a primary output. Hence, regardless of the type of defect, the site where the incorrect logic value occurs must be observed in order for defect detection to take place. The conventional automatic test pattern generator, ATPG, stops at 100% SAF coverage so that not all fault sites are observed enough times to ensure sufficient detection of non-target defects. However, multiple observation of each fault site usually requires a bigger test set size. Since different test sets are formed by different bit assignments, the bit assignment of a test set which detects this defect, are required for this defect's excitation or observation. In this paper, we will present a method to determine the role of each bit of the ATPG test set, and based on the bit assignments, we generate high qualify patterns which guarantees multiple deterministic observation and random excitation of all the fault sites in the circuit.

II. Prior Work

We have shown that increasing the number of observations of the least observed sites can significantly improve defect detection in industrial circuits [1]. In addition, Ma *et al.* showed that a test set that detected all stuck-at faults at least 15 times at speed had no test escapes for the circuits studied [2]. However, multiple observations of circuit sites are often less effective if those observations occur under very similar circuit conditions—especially as defects become more difficult-to-detect and more excitation conditions must be satisfied fortuitously. Trying to reduce the test cycle duration and the complexity of the test setup, some researchers had used pseudo-random patterns in a BIST methodology to test faults in circuits, [3] and [4].

Other researchers proposed a new ATPG algorithm to find a near-minimal test pattern set that detects faults multiple times and achieves excellent defective part level [5]. Furthermore, the author of [6] investigated weighted random patterns generated with partial fault targeting and showed their effectiveness at fortuitous detection. However, to generate the higher quality patterns which guarantee to excite or observe a target fault, we will identify the role of each bit plays in the fault excitation and observation.

III. Excitation and Observation Bits Separation

We start by generating new tests online to allow problems due to defects and wear-out to be detected. Specifically, we generate the fault lists for the circuit c432 and c499 from their verilog files, and the test sets that will detect each fault of the circuit at least 15 times by the ATPG tool. Faults that are detected exactly 15 times are hard faults. Those 15 patterns that detect each hard fault constitute the original pattern list for that hard fault. Therefore, we have H original pattern lists, where H is the number of hard faults. For convenience, we gather all the patterns in these H original pattern lists into a huge test set list, called initial pattern list, which contains (15*H) patterns. Thus, every 15 consecutive initial patterns target the same hard fault. We are trying to find out the excitation and observation bits from each initial pattern for the circuits c432 and c499.

The bits of each pattern are the input of the circuit, which are set to 1, 0 or 'X'. To determine the role each bit plays in fault detection, each bit of each initial pattern is either linearly reversed if it was 0 or1, or kept as it was if it was 'X'. The change of each bit forms a new pattern, and each initial pattern extends N new "reversed" patterns, where N is the input number of the circuit. For the circuit c432, N=36; for the circuit c499, N=41. These N new patterns are simulated to determine if they still detect the targeted hard fault, or they detect another stuck-at fault which shares the same site with the targeted hard fault. There are three possible situations:

1. If the new pattern with one bit changed can still detect the hard fault, the changed bit is not required for the fault observation or excitation, and thus we can change this bit to 'X';
2. If the new pattern cannot detect the hard fault which was detected by the original pattern without the bit changed, but detect another stuck-at fault at this site, then this bit is an excitation bit, but not an observation bit;
3. If the new pattern detects none of the faults at this site, this bit is an observation bit.

In this way, the excitation and observation bits are identified in each pattern, and the bits which are not identified are filled with X's.

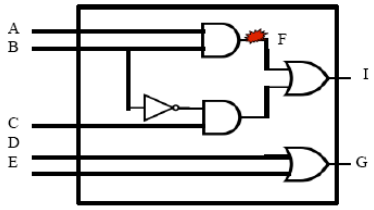


Figure1. Example circuit for targeting "F stuck-at 0".

For example, consider the circuit in Figure 1, with the inputs, "A", "B", "C", "D", "E", and the outputs, "I", "J". Assume that we want to target a stuck-at zero fault on "F". From the patterns corresponding to the fault, "F stuck-at 0", we pick one initial pattern, 111XX, as an example. Four inputs are assigned values, and two are "don't cares". However, all of the assigned bits do not perform the same function. We linearly reverse the bits from the left to right. Hence, 5 new patterns are extended from the initial pattern as shown in Figure 2.

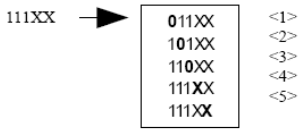


Figure 2. pattern bit exchange example

We re-simulate the new outputs corresponding to these 5 new patterns under the good circuit state, and then test the targeted fault with the new patterns. For pattern <1>, when A=0, F=0 in the good circuit. The fault, "F stuck-at 0", will not be detected. However, the fault, "F stuck-at 1", will lead the output I=1, which should be 0 in the good circuit. Hence, the new pattern <1> misses fault, "F stuck-at 0", but detects the other fault of this site, "F stuck-at 1". This indicates that the first bit of the initial pattern is an excitation bit, but not an observation bit. For pattern <2>, when B=0, F=0 and G=1, so that the output I is always equal to 1. Hence, no matter what the value F is stuck-at, it will never be observed any more. Therefore, pattern <2> could detect neither "F stuck-at 0" nor "F stuck-at 1", which implies the second input of the initial pattern is an observation bit. In this approach, we can infer that the third bit is not required for observation or excitation, and thus we can change it to 'X'. The last two bits are kept as 'X's.

Consequently, one excitation bit and one observation bit are found out from the initial pattern. The rest three are "don't cares". Then, the template with observation bits is: X1XXX; the template with excitation bits is: 1XXXX.

In this example, the fault "F stuck-at 0" is not a hard fault, and there are more than 15 patterns can detect this fault. However, in our experiment, both the circuit c432 and the circuit c499 have hard faults, and each of them has 15 corresponding patterns. We then have 15 different templates including excitation bits and 15 different templates including observation bits for each hard fault. We call them templates excitation/observation-bit templates respectively.

Because in the initial pattern list, every 15 consecutive patterns target the same hard fault, we linearly change the bits at the same position of every 15 consecutive initial patterns at the same time, from the left to right. Hence, we expand (N*15) numbers of new patterns for each targeted hard fault. The whole initial pattern list expands to a "reversed" pattern list, which includes (N*15*H) numbers of new "reversed" patterns. After collecting the hard faults into the hard fault list and, the other stuck-at faults at the same sites into "the other" fault list, we simulate the "reversed" patterns separately through these two fault lists. Then, we transform the two reports into two fault dictionaries, the "hard" fault dictionary and the "the other" fault dictionary. Each of these fault dictionaries is a $H \times (N*15*H)$ matrix, whose row represents the fault in the fault list and column represents the patterns from the "reversed" pattern list. These two matrices only have "1" and "0" elements. "1" indicates the fault of that row detected by the pattern of that column, and "0" means that this fault is not detected by this pattern. In each of these two matrices, the Mth (15*N) consecutive elements of the Mth row correspond to the Mth (15*N) consecutive patterns in the "reversed" pattern list and target the Mth fault in the fault list, for $0<M<H+1$ and $M \in \mathbf{N}$. In the Mth sequence of (15*N) consecutive elements, the Kth 15 consecutive elements correspond to the Kth bits of the original 15 patterns which target the Mth hard fault in the hard fault list. Following the three possible situations, the role of each bit of every pattern in the initial pattern list is identified by comparing these two fault dictionaries. Overall, we get (15*H) excitation-bit templates and (15*H) observation bit templates. The geometry relation between initial pattern list, "reversed" pattern list and the bits of fault dictionary is shown in figure 3.

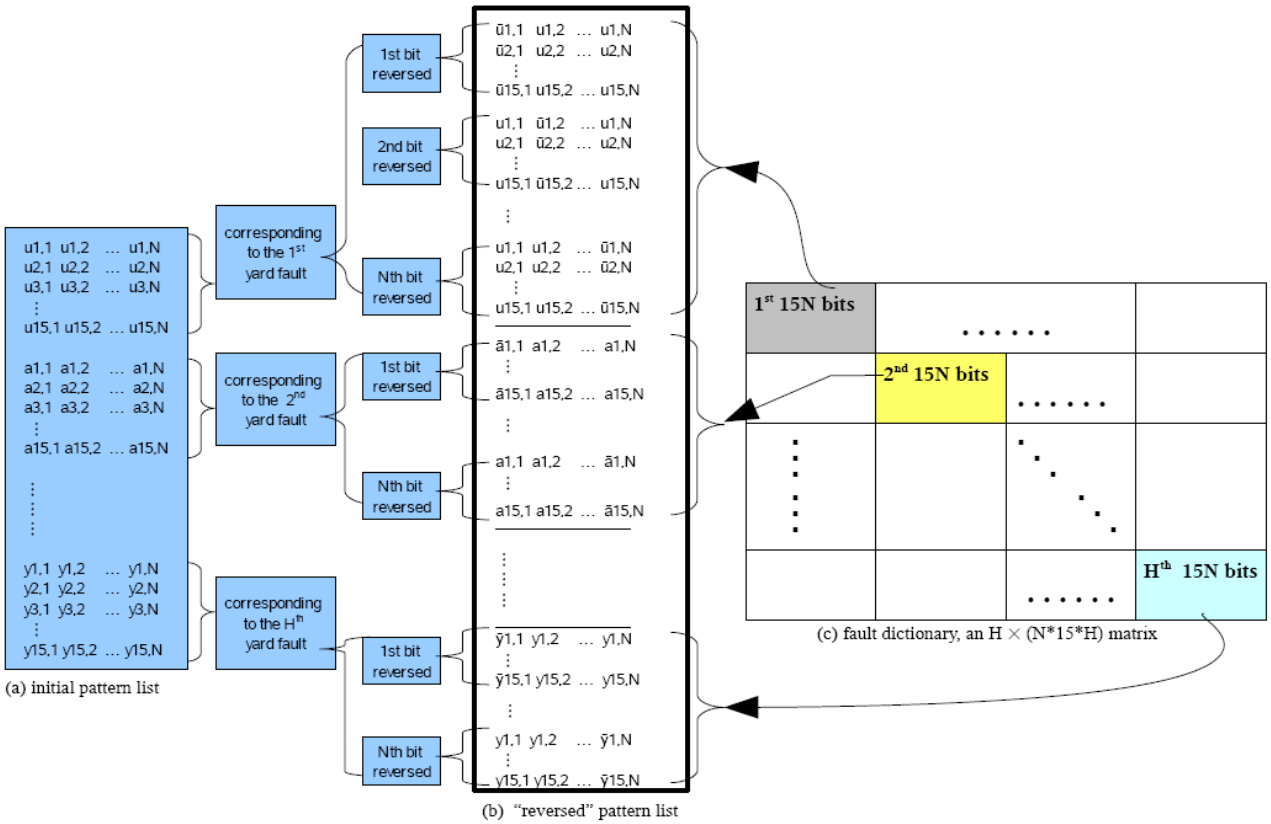


Figure 3. Geometry relation between initial patterns, "reversed" patterns and elements in fault dictionary

IV. Generation of Excitation and Observation Patterns

Although those excitation/observation-bit templates obtained include all the absolute excitation/observation bits, these templates are not precise enough to excite/observe their targeted hard faults. In the last procedure, we inverted every bit linearly in each pattern. However, some bits may be required for both excitation and observation. This deficiency is also visible in the "three possible situations" analysis. The second situation guarantees that the bits in the excitation templates are only required for excitation. However, the third situation cannot guarantee that the observation bits generated are only required for observation, but not required for excitation.

In addition, in some cases, the excitation/observation requirements may be satisfied by alternative bit assignments. For example, the pattern XX01X0 can excite the fault, as long as either the third or the forth bit equal to 0. Because each bit is considered independently in the procedure of section III, we miss this situation. As a result, the final templates generated may miss some bits required for excitation/observation. Thus, to generate high quality excitation/observation patterns which are guaranteed to excite/observe their targeted hard faults, we cannot concern each bit independently.

To solve the bits' double identities and the alternative bits assignments problems, we consider each bit in a new pattern which is generated depending on the role of the last bit. To generate the excitation/observation patterns which are guaranteed to excite/observe their targeted hard faults of the circuits c432 and c499, we use the same initial pattern list as section III.

1. Generating Excitation Patterns

To generate a excitation pattern from a original pattern corresponding to the hard fault, (let's say "P stuck-at 0", denoted by "P/0"), we use an analysis with N steps:

***Step 1*:** simulate the good circuit with the 1st bit of the original pattern changed to 'X', and then see what value the P is;

Case 1: if P/1, then the 1st bit is not required for the fault excitation. We keep it as 'X'.

Case 2: if P/0 or P/X , which means the 1st bit is required for the fault excitation, we then change it back to what it was.

Step 2: simulate the good circuit with the 2nd bit of

the pattern, which is generated from the last step, changed to 'X', and then see what value the P is;

Case 1: if P/1, then the 2nd bit is not required for the fault excitation. We keep it as 'X'.

Case 2: if P/0 or P/X, which means the 2nd bit is required for the fault excitation, we then change it back to what it was.

…

Step N: simulate the good circuit with the Nth bit of the pattern, which is generated from the last step, changed to 'X', and then see what value the P is;

Case 1: if P/1, then the Nth bit is not required for the fault excitation. We keep it as 'X'.

Case 2: if P/0 or P/X, which means the Nth bit is required for the fault excitation, we then change it back to what it was.

After the N steps, we generate an excitation pattern from one original pattern. In each of these N steps, there are two cases to decide if the bit is required for excitation or not. Each of these N steps is to change the relevant bit from a pattern generated from the last step, which guarantees that all the preceding bits in this pattern are either 'X' or required for excitation.

For time efficiency, we change the bits at the same position of all (15*H) patterns in the initial pattern list together before running the good circuit simulation on both faults of all targeted hard fault sites. A targeted hard fault site is explained in figure 4. The simulation log reports values of

Figure 4. A targeted hard fault site: Site P can be stuck-at either 0 or 1, which are each a fault of F. The targeted hard fault could be P stuck-at 0, while the other non-targeted fault is P stuck-at 1. Picking P as the site of interests, P is called the targeted hard fault site.

all targeted hard fault sites corresponding to each of these (15*H) patterns with the same bit in each pattern was changed to 'X'. For each site, we only consider 15 corresponding patterns among all these (15*H) patterns with one bit changed. Following the 2 cases analysis in the every step, we decide whether we change the relevant bit or not. Keeping the bits assignment in all patterns, we change the next bit at the same position of all patterns to 'X', before running the good simulation. Since all the patterns have N bits, the good circuit simulation for analyzing the bits' identities would be run for N times. We implement the process in a loop:

```
for (n=0; n<N; n++){
        change the nth bit of all (15*H) patterns to 'X';
        simulate the good circuit with the whole pattern list;

        report data into the log file;
        log file analysis ();
}
output final pattern list ();
```

```
log file analysis (){
      begin =0;
      for ( hardfault=0; hardfault<H; hardfault++){
         for (pattern=begin; pattern< (begin+15); pattern++){
                fgets(one data line);
                if (P/0 || P/X) change this nth bit back;
                else keep it as 'X';
         }
               begin = begin+15;
      }
}
```

The output pattern list includes high quality excitation patterns which are guaranteed to excite the targeted hard faults.

2. Generating Observation Patterns

To generate a observation pattern from a original pattern which corresponding to the hard fault, "P/0", we need another N steps analysis:

Step 1: simulate the circuit with the 1st bit of the original pattern reversed, and then see what value the P is;

Case 1: if P/1 or P/0, then the 1st bit is not required for the fault observation. We change it to 'X'.

Case 2: if neither P/0 nor P/1 , which means the 1st bit is required for the fault observation, we then change it back to what it was.

Step 2: simulate the circuit with the 2nd bit of the pattern, which is generated from the last step, reversed, and then see what value the P is;

Case 1: if P/1 or P/0, then the 2nd bit is not required for the fault observation. We change it to 'X'.

Case 2: if neither P/0 nor P/1 , which means the 2nd bit is required for the fault observation, we then change it back to what it was.

…

Step N: simulate the circuit with the Nth bit of the pattern, generated from the last step, reversed, and then see what value the P is;

Case 1: if P/1 or P/0, then the Nth bit is not required for the fault observation. We change it to 'X'.

Case 2: if neither P/0 nor P/1, which means the Nth bit is required for the fault observation, we then change it back to what it was.

Using this N step process, we have generated an observation pattern from the original pattern from the section III. Because of the definition difference between the observation and excitation bit, the two N steps analysis of excitation and observation patterns' generations are different. To be more efficient, we reverse the bits at the same position of all (15*H) patterns in the initial pattern list together before simulating the circuits. In the circuit simulation, we report both the two "stuck-at" faults at the hard fault's sites. The simulation log reports both hard faults and "the other" faults at the same site with the "reversed" patterns which detect these faults. For each site, we only consider the 15

corresponding “reversed” patterns among all (15*H) “reversed” patterns. We use another loop to reverse the bits and, analyze the log file.

```
for (n=0; n<N; n++){
        reverse the nth bit of all (15*H) patterns;
        simulate the circuit with the whole pattern list;
        report data into the log file;
        log file analysis ();
 }
 output final pattern list ();

 log file analysis (){
     for ( hardfault=0; hardfault<H; hardfault++){

        for the hard fault/“the other” fault of this site (ex: P/1):
            while( gets(data) ){
          if (the corresponding patterns detect the fault)
                change this nth bit to 'X';
          if(pin changes) break;
        }
        if(any nth bit !='X') change it back;

        for the “the other” fault/hard fault of this site (ex: P/0):
            while( gets(data) ){
          if (the corresponding patterns detect the fault)
                change this nth bit to 'X';
          if(pin changes) break;
        }

}
```

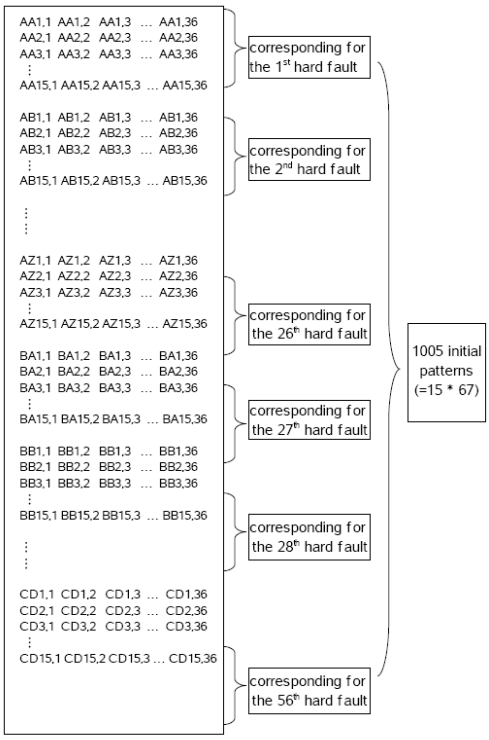
As the pseudo code shows, we scan every 15 corresponding patterns twice for each targeted hard fault site. If the corresponding pattern detects one fault (ex: P/1) at this site, we change the relevant bits to 'X'. Otherwise, we change them back. Then we analyze the other fault (ex: P/0) at the same site. If any of the 15 corresponding patterns, which fail to detect the last fault (ex: P/1), but detect this fault (ex: P/0), the relative bits, which have been reversed back in the last fault analysis, will be changed to 'X'. Therefore, only the bits which detect either the hard fault or “the other” fault at the same site, are changed to 'X'. The resulting pattern list includes high quality observation patterns which are guaranteed to observe the targeted hard faults. This list is called the observation pattern list; every 15 consecutive patterns correspond to each targeted hard fault in the circuit.

To check the excitation/observation pattern list, we compare these excitation/observation patterns with the excitation/observation-bit templates obtained in section III. All the non-'X' bits in the excitation/observation-bit templates should be included in the excitation/observation patterns.

V. Results and Analysis

1. Excitation and Observation Bits Separation

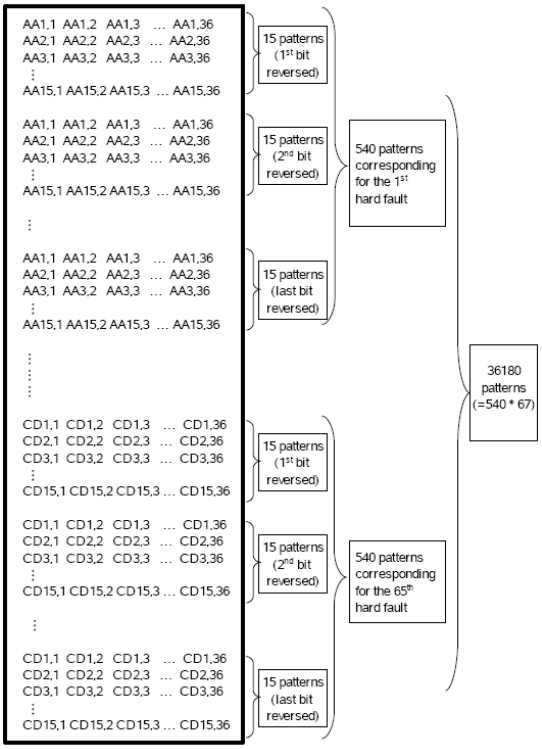
For the circuit c432, 526 test sets which are guaranteed to detect all the faults by at least 15 times, are generated by the ATPG tool through the FastScan program. In the circuit c432, 67 hard faults are detected by these test sets. After gathering all the 15 patterns corresponding to these 67 hard faults into one pattern list, the circuit c432's initial pattern list includes 1005 patterns. Hence, 36180(=1005*36) “reversed” patterns are expanded after linearly reversing the bit of the initial patterns from the left to the right. The format of the initial pattern list and the “reversed” pattern list for the circuit c432 are shown in figure 5(a) and (b) respectively.



(a) initial pattern list of the circuit c432

For the circuit c499, 787 test sets were generated, which detected 170 hard faults. These 170 hard faults totally have 2550 patterns in the initial pattern list. Its “reversed” pattern list includes 104550(=2550*41) new patterns.

After the hard faults simulation and the other faults simulation through the “reversed” patterns, “reversed” patterns were identified as could or could not detect the hard faults or the other faults. Comparing the role the bits played in the hard faults detection with the role the same bits played in “the other” faults detection, we obtained the excitation-bit templates and observation-bit templates through the three possible situations outlined in section III.



(b) "reversed" pattern list

Figure 5. c432 pattern list format

The excitation/observation-bit templates include only absolute excitation/observation bits and 'X' bits. As a result, 1005 excitation/observation-bit templates corresponding to the
1005 initial patterns were generated for the circuit c432; 2550 excitation/observation-bit templates corresponding to the 2550 initial patterns were obtained for the circuit c499. The number of bits, hard faults and corresponding patterns for the circuits c432 and c499 are shown in table 1.

	c432	c499
Input Number	36	41
Hard faults Number	67	170
Initial patterns Number	1005	2550
"Reversed" patterns Number	36180	104550
Excitation bit patterns Number	1005	2550
Observation bit patterns Number	1005	2550

Table 1. Bits, hard faults and pattern number of the circuit c432 and c499

In each paralleled excitation-bit template and observation-bit template, the non-'X' bits generated were different bits, which indicates that the bit of an ATPG set can be only required for fault excitation or only required for fault observation or "don't cares". As we discussed in section IV, some of these observation bits in observation-bit templates are both required for fault excitation and observation due to the bits double identities. However, those double identity bits were not included in excitation-bit templates. Hence, the excitation-bit templates with the absolute excitation bits were not yet the excitation patterns which could be guaranteed to excite all the hard faults. Besides, due to the alternative bits assignments, the observation-bit templates have not included all the bits required for observation yet. Thus, although the excitation/observation bits included in these templates were absolutely required for the targeted hard faults excitation/observation, they were not all the bits required for the excitation/observation.

We counted the non-'X' bits in every 15 consecutive excitation/observation-bit templates which correspond to the same hard fault, and calculated the average number of excitation/observation bits for each targeted hard fault by formula (1). Then, using formula (2), we calculated the mean value of all the average values obtained in formula (1) to get the average number of excitation/observation bits for any hard fault of the circuit.

$$\text{Average Num. of excitation/observation bits for a specific hard fault} = \frac{\sum_{1st\ template}^{15th\ template} (\text{Num. of excitation/observation bits} \in \text{this template})}{15} \quad (1)$$

$$\text{Average Num. of excitation/observation bits for any hard fault} = \frac{\sum_{1st\ hard\ fault}^{Hth\ hard\ fault} (\text{Average Num. of excitation/observation bits for this hard fault})}{H} \quad (2)$$

As a result, for the circuit c432, there were 240 excitation-bit templates corresponding to 16 hard faults, only included 1 excitation bit; the average number of excitation bits across all excitation-bit templates was 2.349.15 observation-bit templates corresponding to 1 hard fault included 1 observation bit; the average number of observation bits across all observation-bit template was 7.393.

For the circuit c499, 589 excitation-bit templates corresponding to 64 hard faults had only 'X' bits, which proved that excitation-bit templates did not include all bits required for excitation. The average number of excitation bits across all excitation-bit templates was 12.751. 480 observation-bit templates corresponding to 32 hard faults did not include observation bits, which proved that observation bit templates did not generate all bits required for observation. The average number of excitation bits across all observation-bit templates was 25.744..

2. Excitation and Observation patterns

Using the same initial pattern lists as shown in figure 5(a), 1005 excitation/observation patterns were generated for the circuit c432; 2550 excitation/observation patterns were generated for the circuit c499.

For the circuit c432, 210 excitation patterns which correspond to 14 hard faults, include 1 excitation bit. All these 210 excitation patterns belong to the group of 240 excitation-bit templates which have only 1 non-'X' bit. The average number of bits required for hard fault excitation across all excitation patterns for c432 was 7.117. The observation patterns included at least 9 bits which were

required for hard fault observation. 150 observation patterns corresponding to 10 hard faults included exactly 9 observation bits. The average number of bits required for hard fault observation across all observation patterns for c432 was 21.424.

For the circuit c499, 908 excitation patterns have the least number of non-'X' bits, 13. The average number of bits required for hard fault excitation across all excitation patterns for c499 was 22.817. 278 observation patterns have the least non-'X' bits, 33. The average number of bits required for hard fault observation across all observation patterns for c499 was 37.918.

Comparing the excitation/observation-bit templates with the excitation/observation patterns, we found all the non-'X' bits in templates were included in the paralleled patterns. None of the excitation and observation patterns included all 'X' bits, which was a reasonable result. The data comparison between the excitation/observation-bit templates and the excitation/observation patterns is shown in table 2.

circuit		c432				c499			
		Excitation bit templates	Excitation patterns	Observation bit templates	Observation patterns	Excitation bit templates	Excitation patterns	Observation bit templates	Observation patterns
Least non-'X bits'	Test sets' number	240	210	15	150	589	908	480	278
	Bits' number	1	14	1	9	0	13	0	33
Average non-'X' bits		2.349	7.117	7.393	21.424	12.751	22.817	25.744	37.918

Table 2. Comparison between excitation/observation bit templates and excitation/observation patterns

The average numbers of absolute excitation and observation bits for each targeted hard fault, and the average numbers of bits required for each targeted hard fault excitation and observation for the circuit c432 and c499 are shown in the Figure 6 and 7 respectively.

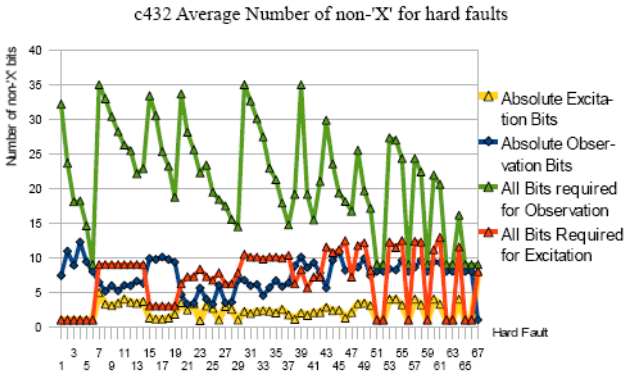


Figure 6. absolute excitation/observation bits and bits required for excitation/observation for the circuit c432

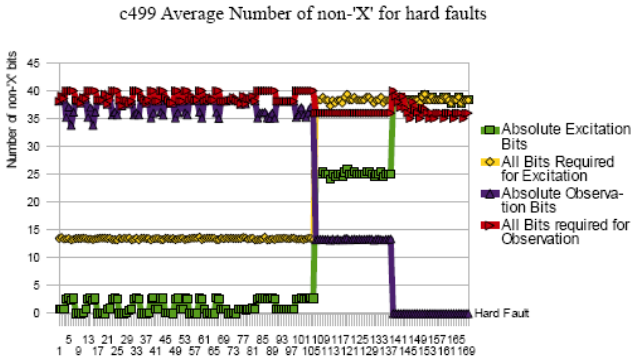


Figure 7. absolute excitation/observation bits and bits required for excitation/observation for the circuit c499

Figure 6 and 7 shows that for both the circuit c432 and the circuit c499, the average number of bits required for each hard fault excitation/observation is more than the average number of absolute excitation/observation bits for that targeted hard fault. Their difference indicates that there exist a certain number of bits in the ATPG sets having double identities or enrolled in alternative bit assignments.

The results of excitation/observation patterns of the circuit c432 and c499 are guaranteed to excite/observe their corresponding hard faults of the circuit c432 and c499, which increases the effectiveness and efficiency of the randomly generated test sets to detect the hard faults.

VI. Conclusion

We have generated patterns which are guaranteed to excite/observe hard faults of the circuit c432 and c499. The excitation/observation patterns can 100% excite/observe the targeted defects without detecting the other ones. They increase the effectiveness and efficiency of the initial patterns, which randomly generated by ATPG tool.

Besides, we also investigated each bit's identity through our three possible situations analysis and N step process. The non-'X' bit in excitation/observation bit templates are absolute excitation/observation bits independent on the other bits. The extra non-'X' bits included in the excitation/observation patterns are the excitation/observation bits having double identities or depending on the other bits.

VII. Reference

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