Testing Timing Delays on FPGA's to Compare with the Timing Delay of an ASIC in a 3D IC

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ABSTRACT

In this paper I describe how and why I tested the timing delay of FPGA's. Also I describe what kind of tools I used to collect data. This paper is part of a larger project that is trying to determine how much performance will be lost by re-routing logic through an FPGA from a broken piece of logic in an ASIC. We are also trying to determine if an inexpensive FPGA will be feasible in the timing delays compared to an ASIC.

Keywords
TSV, 3D IC, FPGA, ASIC, Delay

1. Introduction

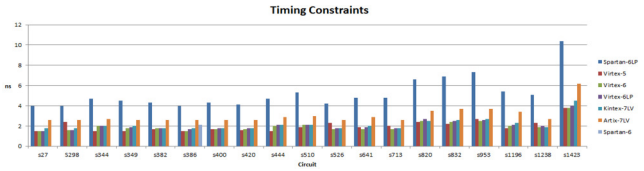
Usually when a 3D IC is defective the whole chip is discarded which could be very expensive. One alternative is to re-route the logic from the broken ASIC through an FPGA which would already be in the 3D stack. I will gather data on several FPGA's currently available on the market. I will gather timing constraints so we can compare them with the timing constraints of an ASIC. I will also gather the prices of the FPGA's. I will also discuss what other research needs to take place to complete the project.

2. Data

I gathered timing constraints for several Xilinx FPGA's including Artix, Spartan, Virtex, and Kintex on a variety of circuits. The Artix FPGA's are new to the market so they did not include a price. The new Artix FPGA boasts to be less expensive and consume less power than similarly priced FPGA's. The least expensive FPGA's belong to the Spartan family. The Spartan family of FPGA's is also the slowest of all the FPGA's I tested.

I used a Xilinx simulation tool to test all of the FPGA's. Xilinx Design Suite 14.1 was the newest version of the simulation tool they had. After a little help from my research partner I was ready to gather data on the FPGA's. Figure 2.1 shows some of the timing constraints of different FPGA's

Figure 2.1



As you can see the Spartan Family of FPGA's is the slowest of all the FPGA's tested. The Spartan Family of FPGA's is also the least inexpensive of all the FPGA's tested as you can see in Figure 2.2

Figure 2.2

Family	Device, Speed, Package, Grade	Device Logic Cells	Process Technology	Price USD
Spartan-6LP	XC6SLX4L, -1L, TQG144, C	3,840	45 nm	$11.81
Virtex-5	XC5VLX20T, -2, FF323, C	?	65 nm	$301.33
Virtex-6	XC6VCX75T, -2, FF484, C	74,496	40 nm	$510
Virtex-6LP	XC6VLX75TL, -1L, TQG144, C	74,496	40 nm	$663.75
Kintex-7LV	XC7K70TL, -2L, FBG676, C	65,600	28 nm	?
Artix-7LV	XC7A100TL, -2L, CSG324, C	101,400	28 nm	?
Spartan-6	XC6SLX9, -3N, FTG256, C	9,152	45 nm	$16.94

The prices vary from Family to Family and also on the speed, grade, and amount of logic cells. As stated earlier the Artix Family is new to the market and does not have a price yet. Figure 2.3 shows the ordering info for the FPGA's

Figure 2.3

The Artix-7, Kintex-7, and Virtex-7 FPGA ordering information, shown in Figure 1, applies to all packages including Pb-Free. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

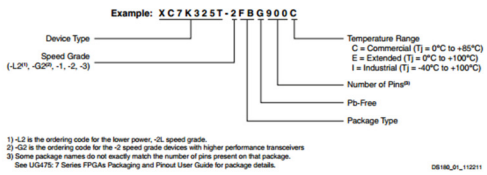


Figure 1: **Ordering Information**

I also gathered data on different speed grades and the low voltage package on the Artix and Kintex family of FPGA's. The data is shown in Figure 2.4 and 2.5 respectively.

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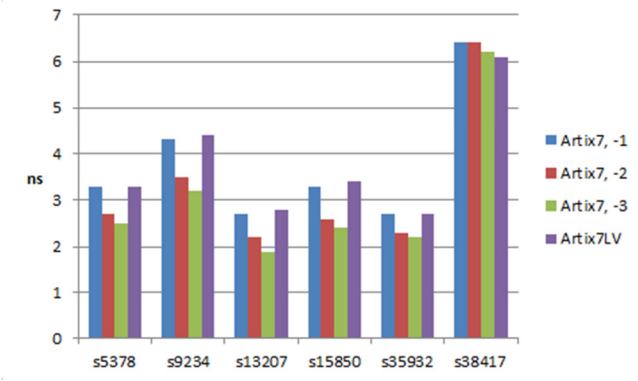

Fig. 2.4. Artix Family of FPGA's in three different speed grades and low voltage packages. All timing is in Nano seconds.

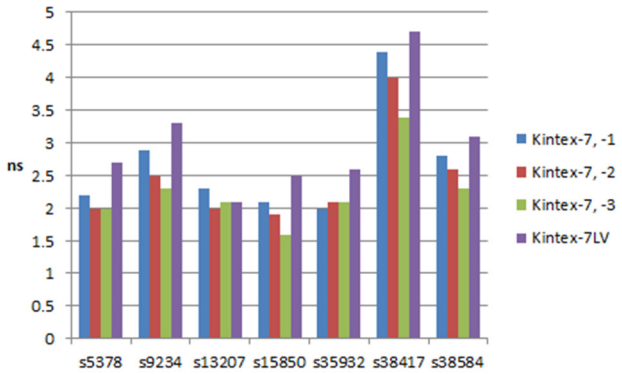

Fig. 2.5. Kintex Family of FPGA's in three different speed grades and low voltage packages. All timing is in Nano seconds.

The data is gathered to compare with the timing of an ASIC. If the timing delay is not a major factor and the price is within range of what the manufacturer will be willing to spend on a back-up plan for their ASIC; the technology will be feasible. Our application will most likely be used by the occasional computer user. Although the research can also be used for other applications, it all depends on what types of delay are acceptable in certain applications. The most logical application would be for the home computer user who occasionally uses their computer to check e-mail, surf the web, access social media, and do some shopping.

3. Future Work

The data for the timing delay of the ASIC will have to be gathered to compare with the data I collected. The data for the ASIC is collected using the **Synopsys** tool. We will also have to look at the capacitance created by the TSV. The more TSV's used the higher the capacitance and the longer the delay. Also, buffers will have to be inserted in front and back of the TSV's to decreases the timing delay of the 3D IC [1]. 2D IC is sometimes faster than 3D IC, especially when small circuits are used. The size of the circuit depends on the process technology, how the buffers are inserted, and the number of dies in the stack. As long as the circuits are large we shouldn't have a problem with the 3D IC performing slower than a 2D IC.

Partitioning the circuit is also needed to maximize the performance of the 3D IC. Tools like **Hmetis** can be used to help in the partitioning process. We must also remember to factor in the capacitance and resistance of the TSV's when partitioning the circuit.

Power consumption will also be a factor when determining which FPGA to use. Power consumption is always a factor in 3D IC because of the heat generated by the dies. Even if the buffers insertion is correct and power consumption is low we should still consider using low power or low voltage FPGA's.

4. Conclusion

The goal of this research is to save money by preventing 3D IC's from being discarded because of faulty logic in the ASIC. As technology advances in the development of FPGA's this research will become more relevant. FPGA's are becoming faster, smaller and more powerful; enabling many different applications to use a FPGA to re-route broken logic in their ASIC.

5. References

[1] D. H. Kim and S. K. Lim, "Through-Silicon-Via-aware Delay and Power Prediction Model for Buffered Interconnects in 3D ICs" *SLIP' 10*, June 13, 2010, Anaheim, California, USA pp. 25-31.