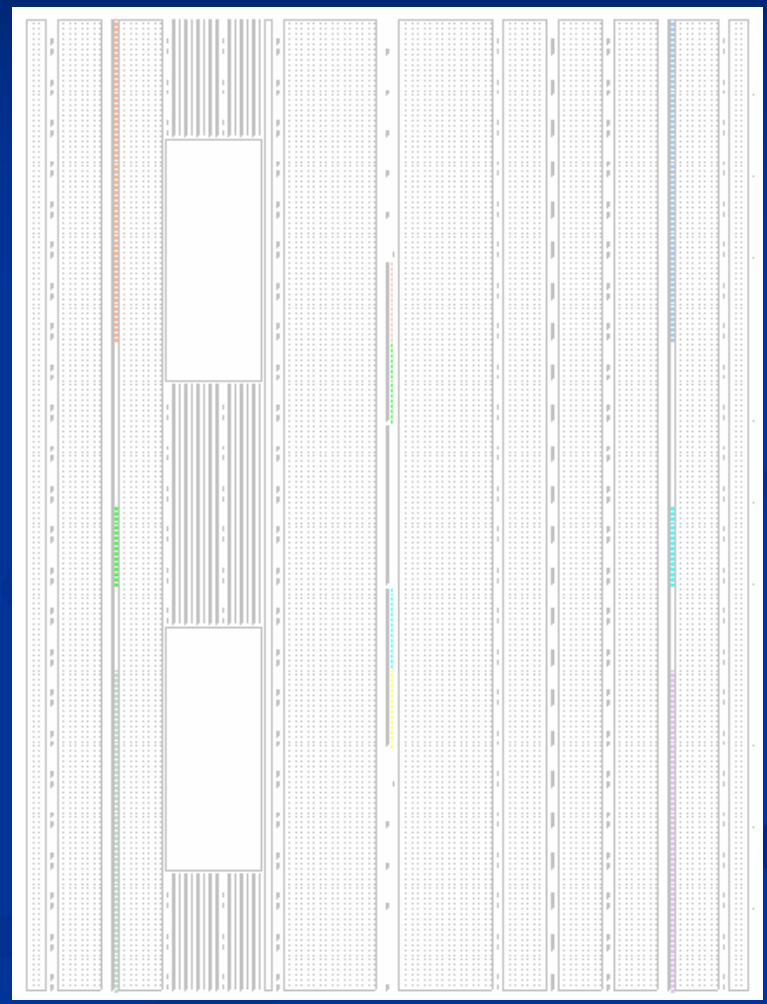
Module Placement during FPGA Partial Reconfiguration

Jin Hu

August 10th, 2005

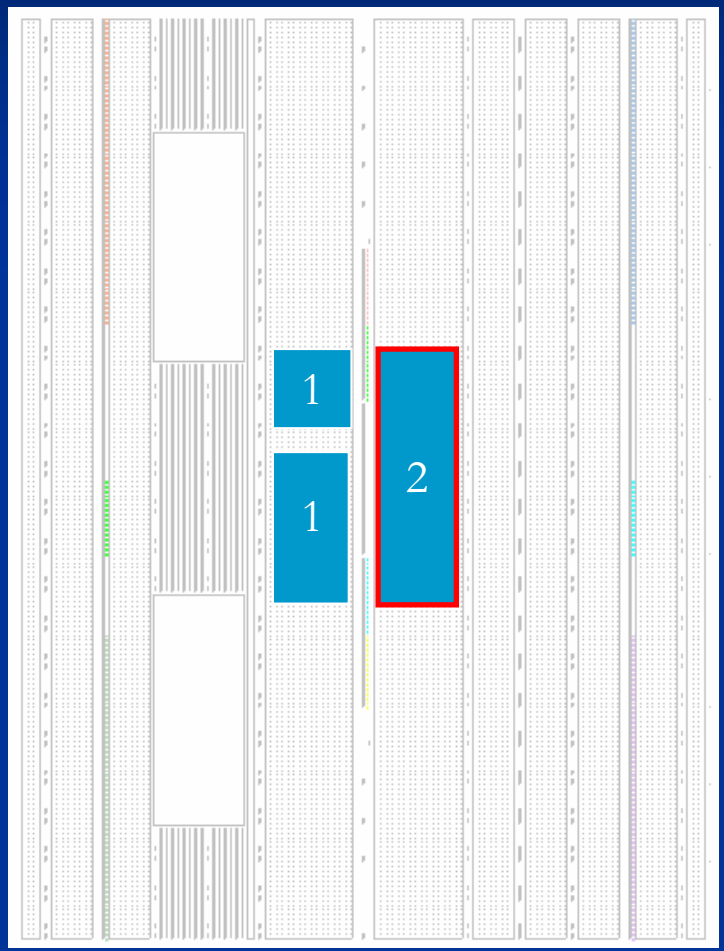
Outline

- **Project Overview**
  - Introduction
  - Big Picture
  - Motivation
  - Description
- **Accomplished Work**
  - Module Placement
    - 32-Bit Multipliers
    - 32-Bit Multiplier-Adders
  - Interface
    - 32-Bit Multiplier Plus Wrappers
- **Future Plans**
  - Dataflow Graphs
  - White Space Estimation
- **Conclusion**

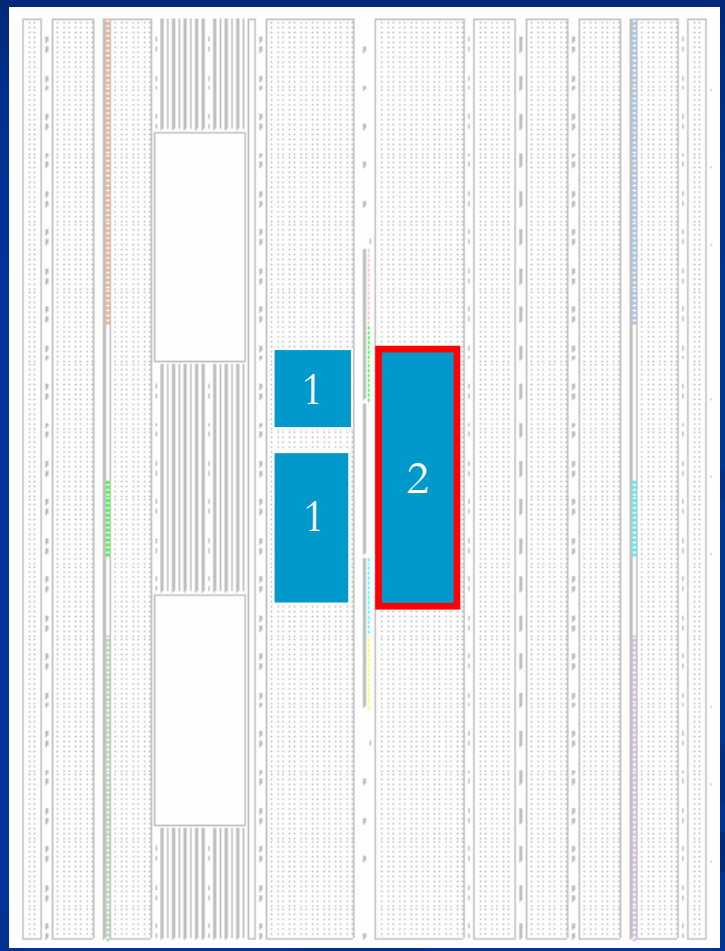


FPGA Virtex-4™ Board

Introduction



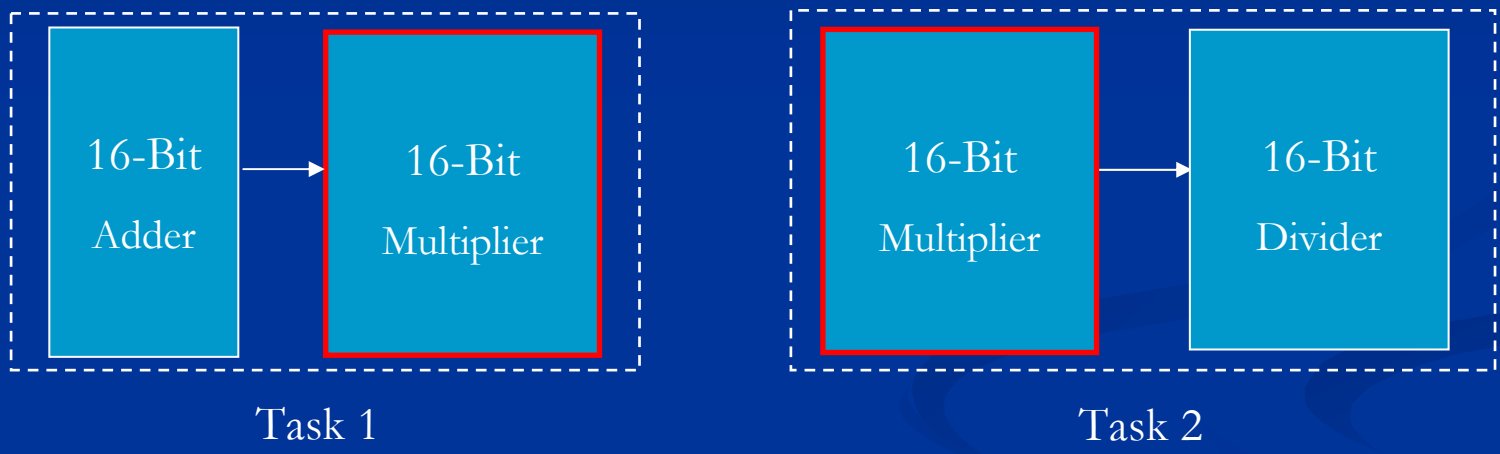
No Partial Reconfiguration



With Partial Reconfiguration

Big Picture

- Different tasks can have repeating components



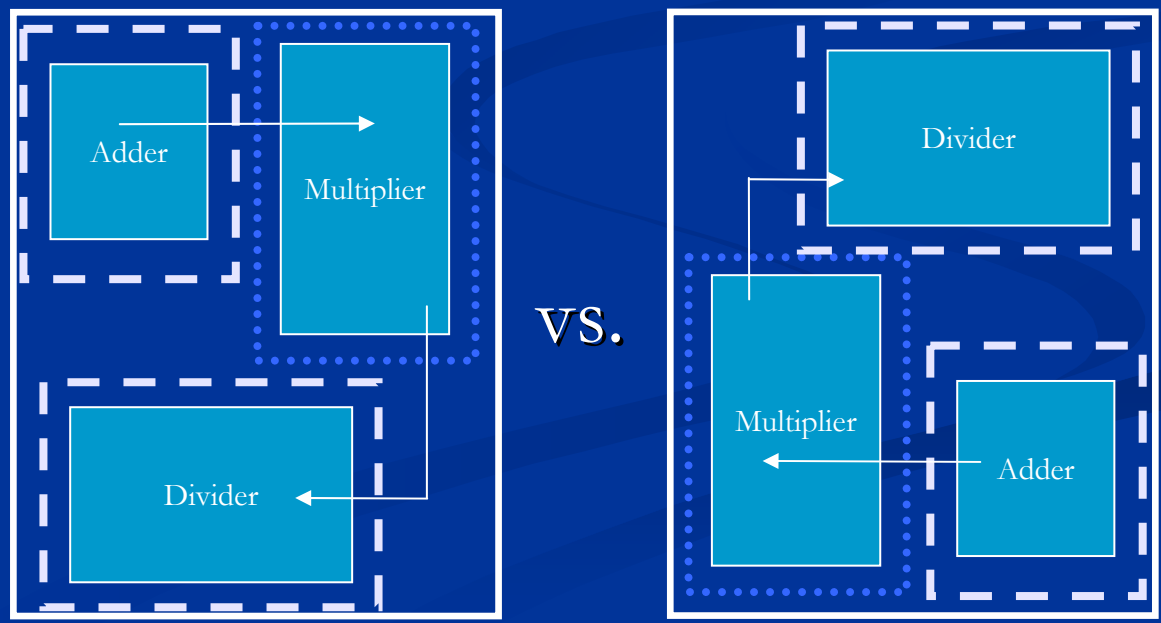
- Partial reconfiguration decision criteria
  - Time
  - Frames and Bits: $1\,\text{Frame} \times \frac{40\ \text{words}}{1\,\text{Frame}} \times \frac{4\ \text{bytes}}{1\ \text{word}} \times \frac{8\ \text{bits}}{1\ \text{byte}} = 1280\ \text{bits}$

Motivation

- Take advantage of common components
- Cheaper than completely reprogramming
- Combination of static and dynamic programming

Description

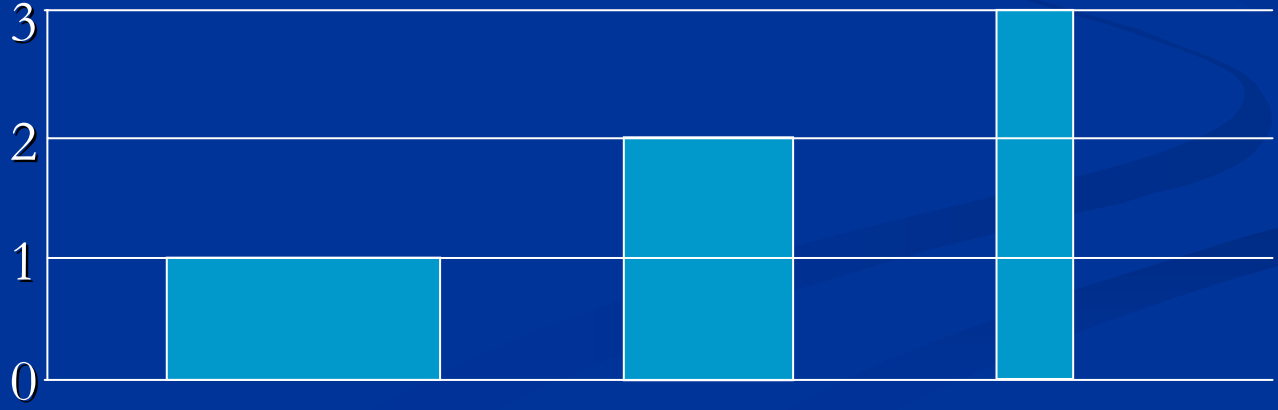
- Given a sequence of tasks, place logic such that bit reconfiguration is minimized
- Considerations
  - Module placement
  - Interface



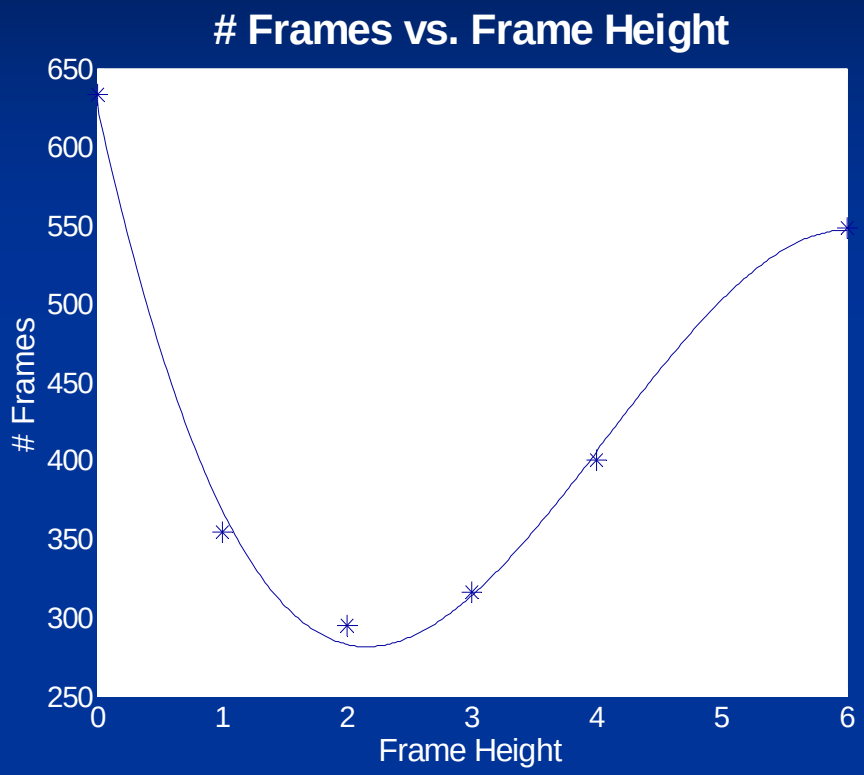
Module Placement

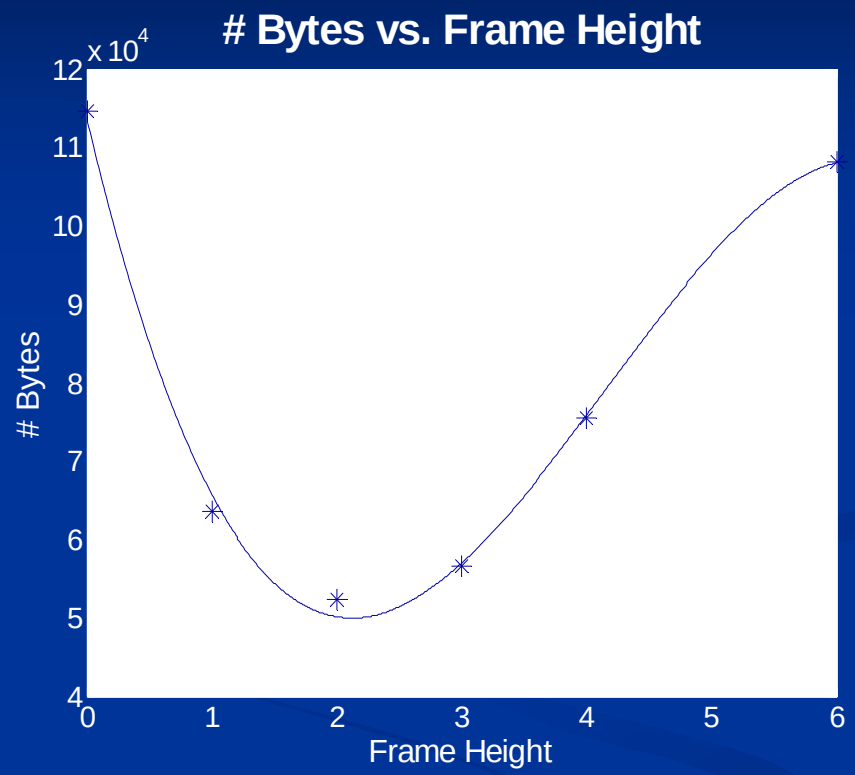
- Module Definition

- Optimal sizing of modules
  - Flexibility of shape
  - Minimize # of frames and bits



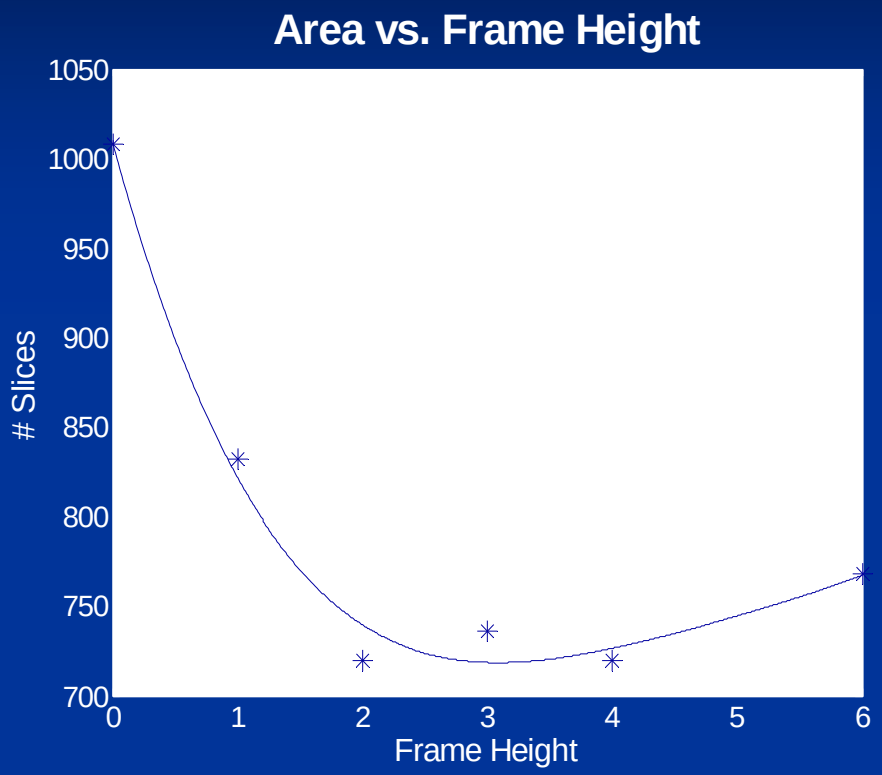
32-Bit Multipliers

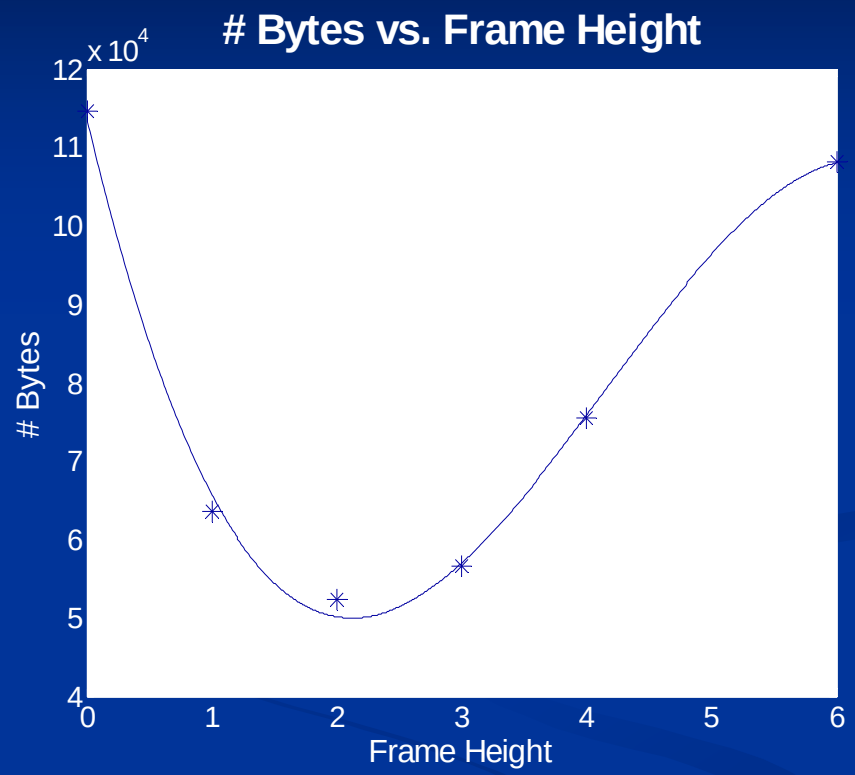




- Frames and bytes relationships similar
- Implies predictable pattern

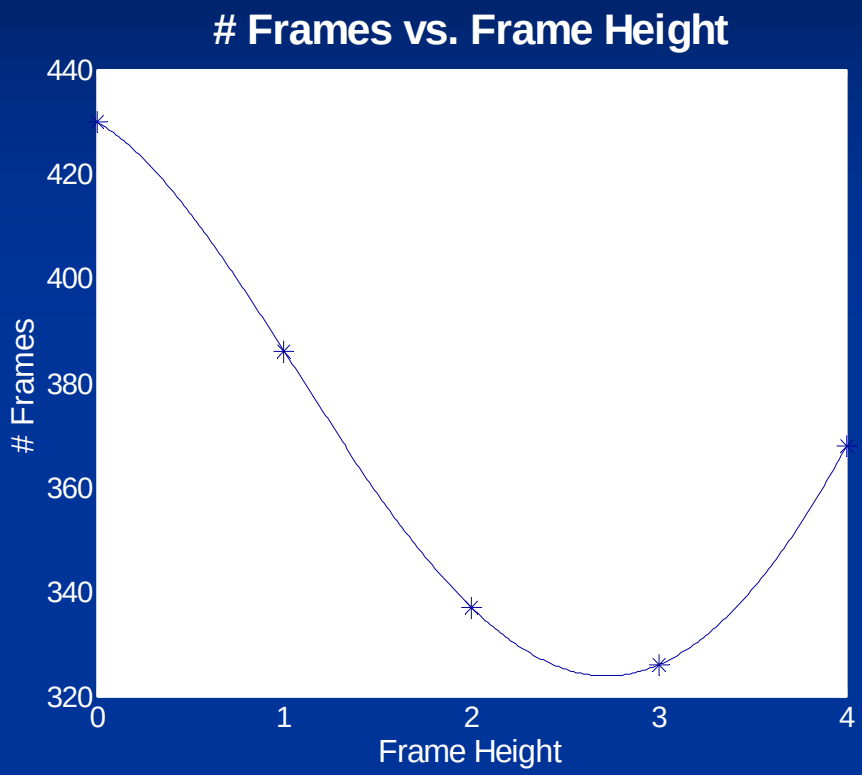
32-Bit Multipliers

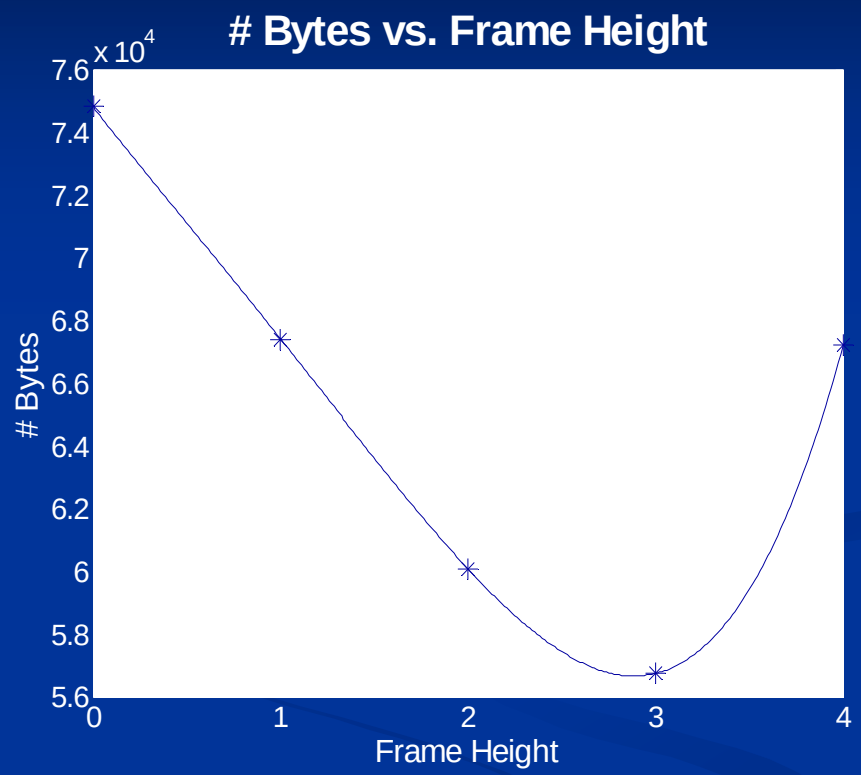




- Area and bytes relationships not similar
- Area stays relatively constant while bytes increase

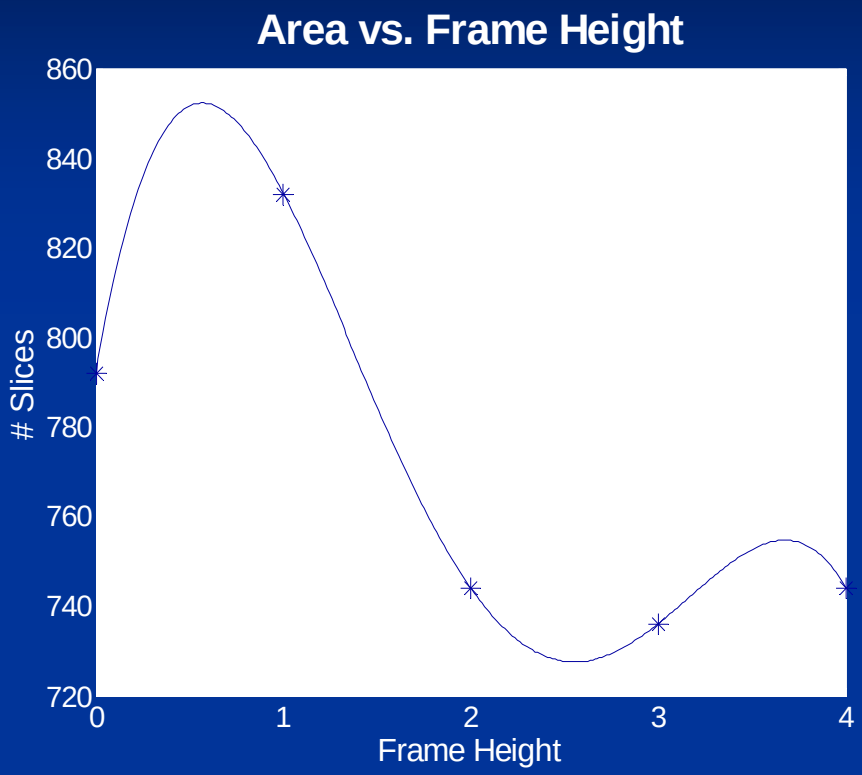
32-Bit Multiplier-Adders

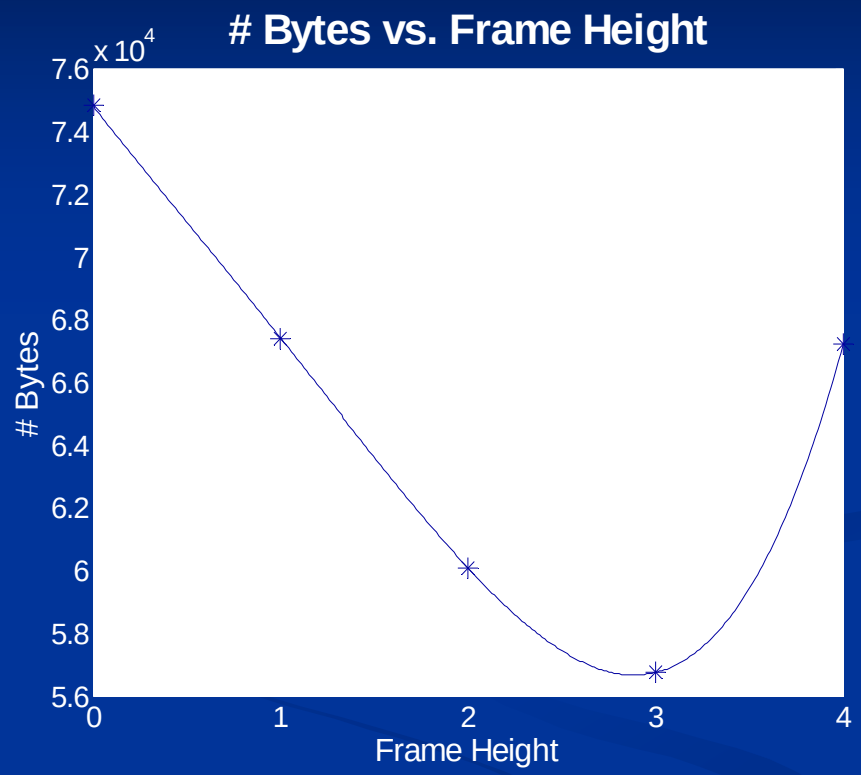




- Relationships for frames and bytes similar
- Correlation similar to multiplier only trends

32-Bit Multiplier-Adders

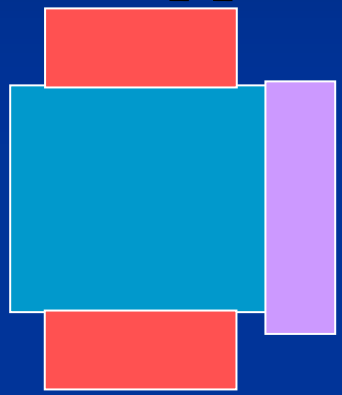




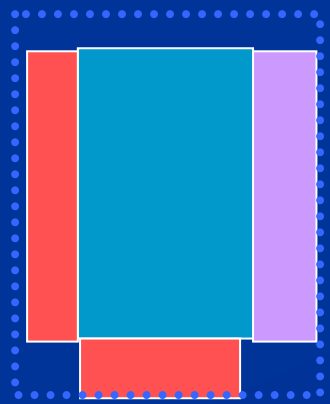
- Area and bytes relationships not similar
- No clear pattern between area and bytes

Interface

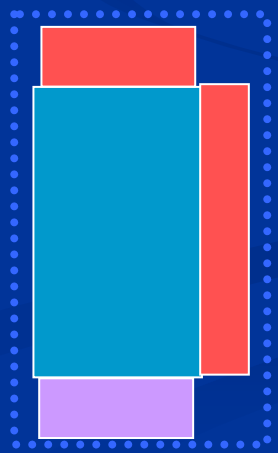
- Fix interface with wrappers

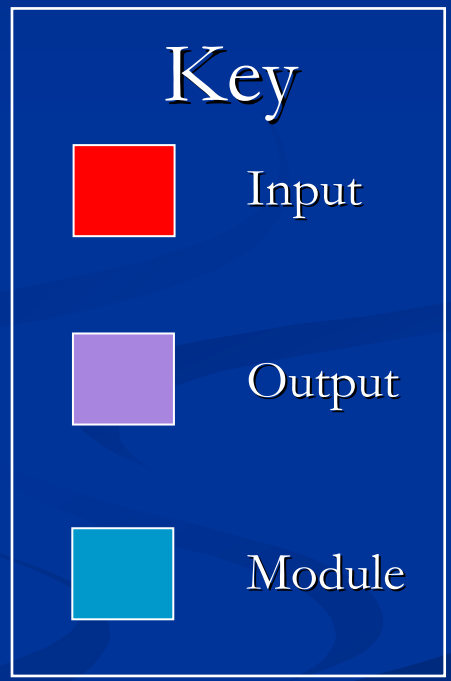


- Wrappers are moveable

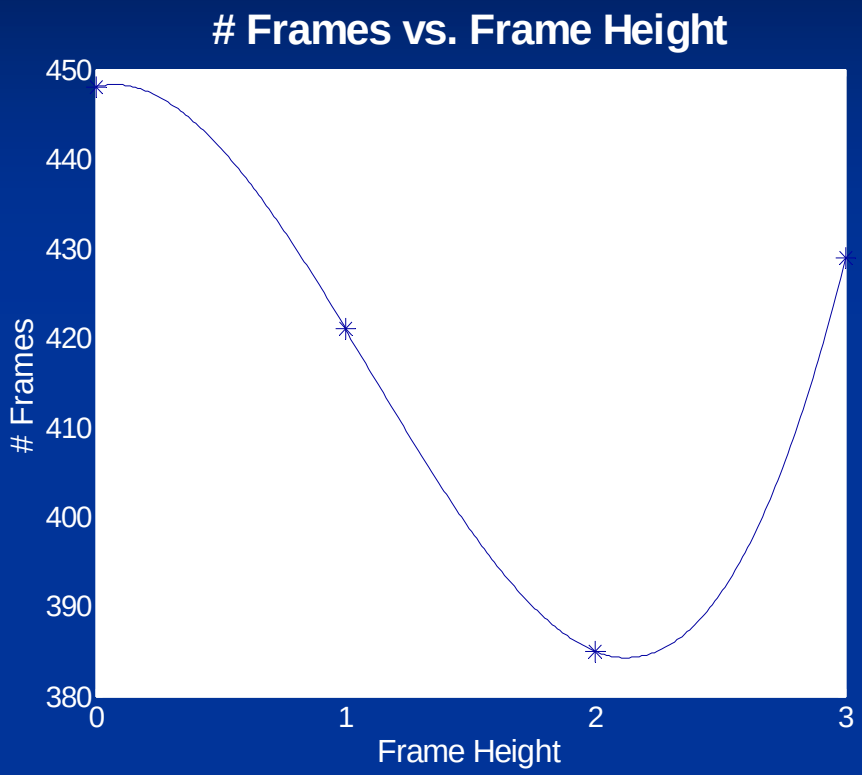


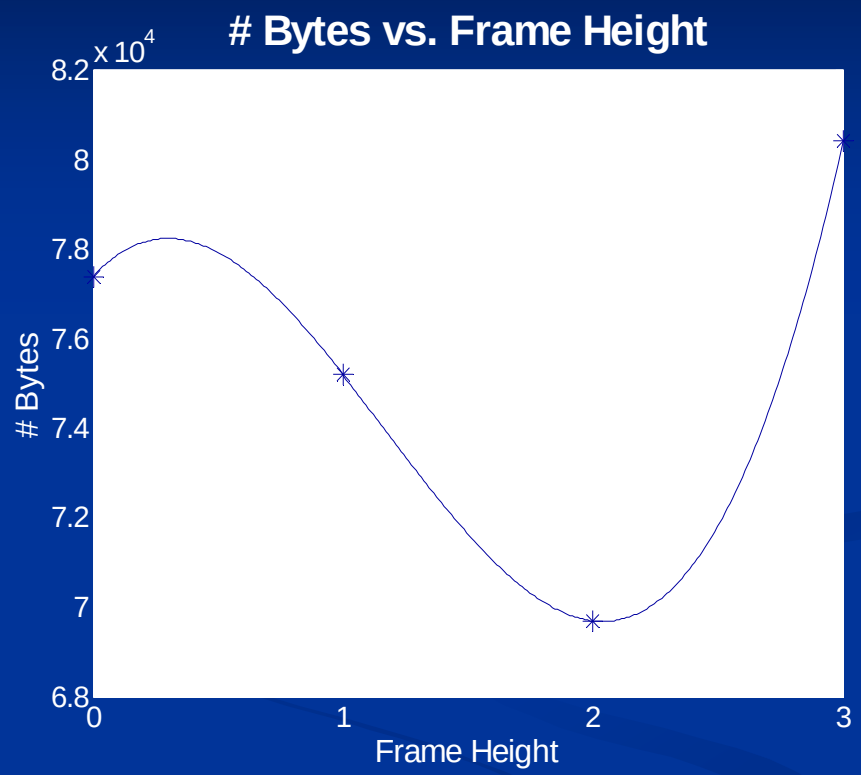
vs.





32-Bit Multiplier Plus Wrappers

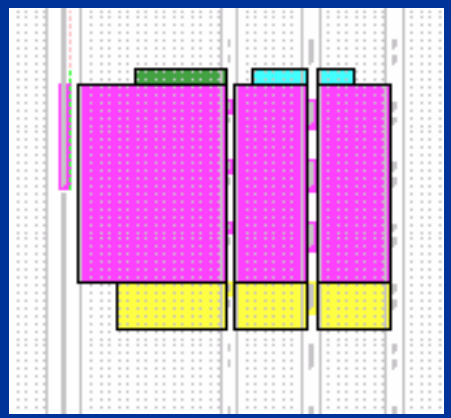




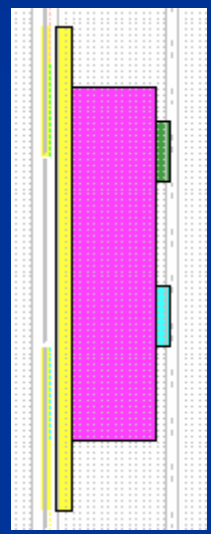
- Frames and bytes relationship not as close as before
- More variation when establishing patterns

32-Bit Multiplier Plus Wrappers

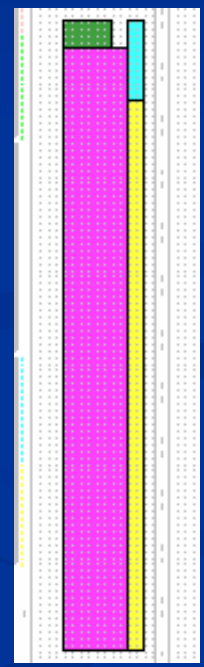
- Optimal Best Arrangements



- Frame Height: 1
- # Frames: 406
- # Bytes: 71,291



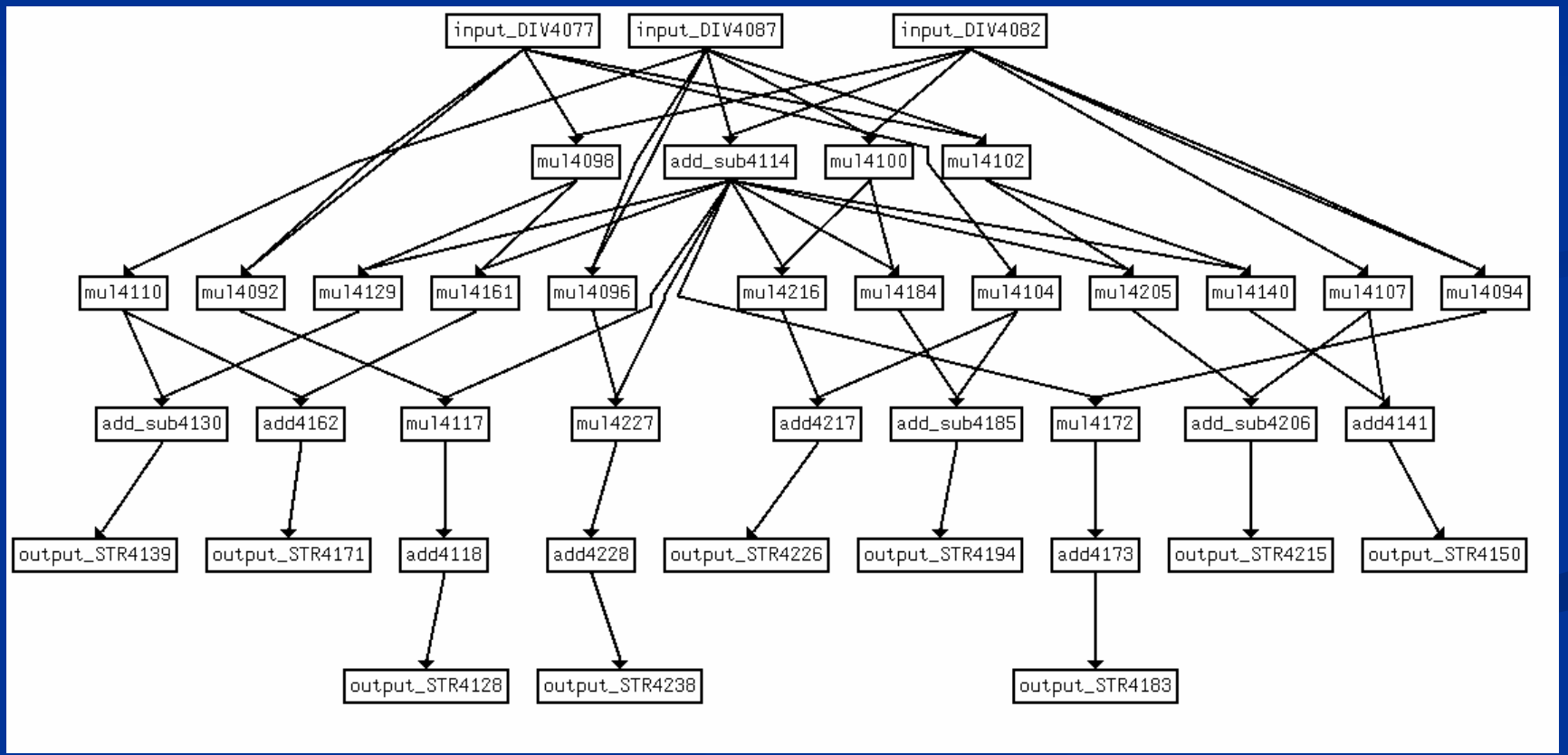
- Frame Height: 2
- # Frames: 355
- # Bytes: 63,731



- Frame Height: 3
- # Frames: 406
- # Bytes: 72,723

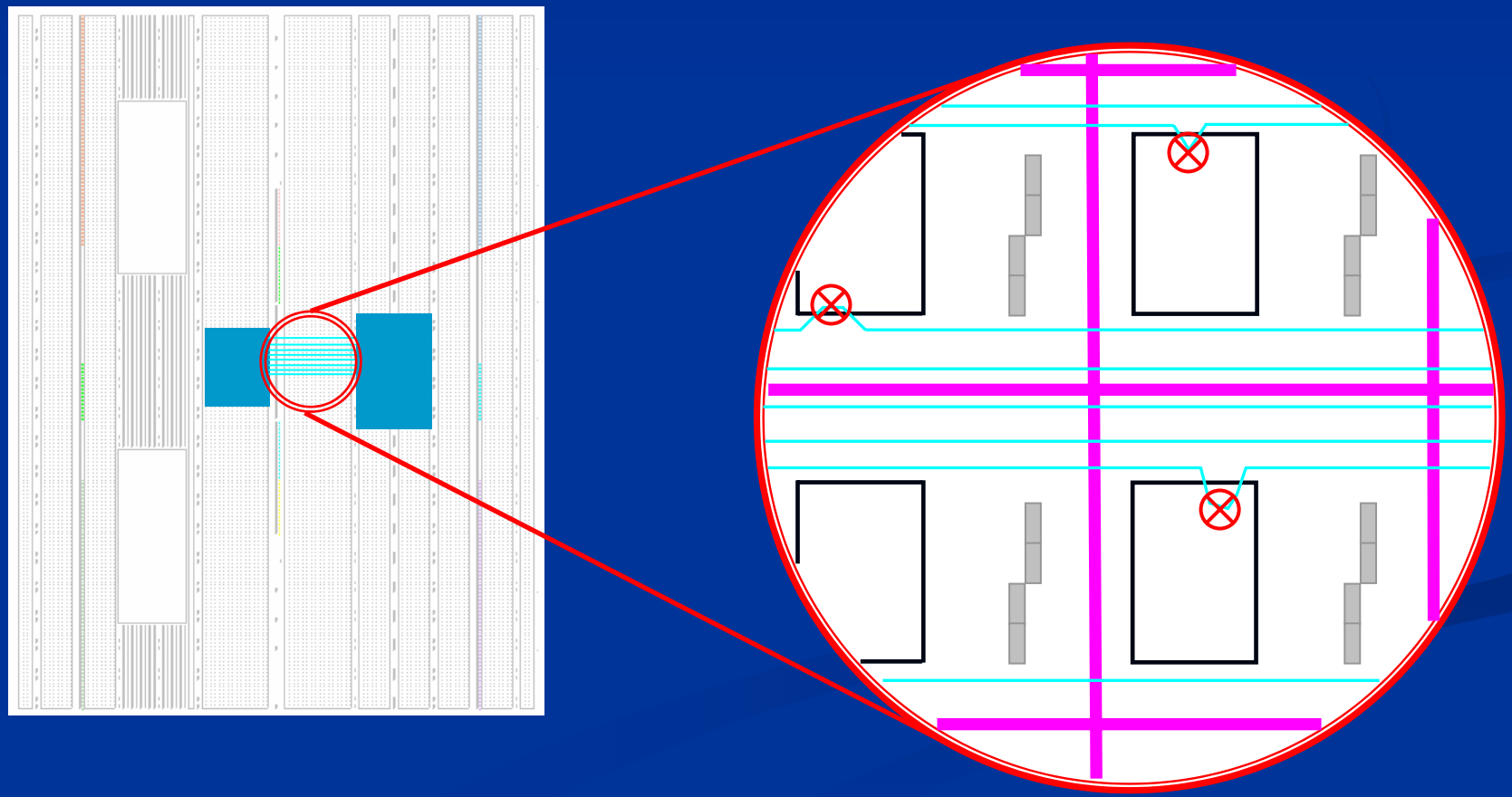
Dataflow Graphs

- Implement designs based on applications



White Space Estimation

- How much does routing cost?



Conclusion

- Goal: Minimize number of bits to reconfigure
- Maximize usage of frame height
- Contiguous components have strong frame to byte relationship
- Any Questions?