Module Placement during FPGA Partial Reconfiguration

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  - Constrained
  - Constrained with Interface
  - Full vs. Partial Mapping
- **Future Work**
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  - Systematic Layout
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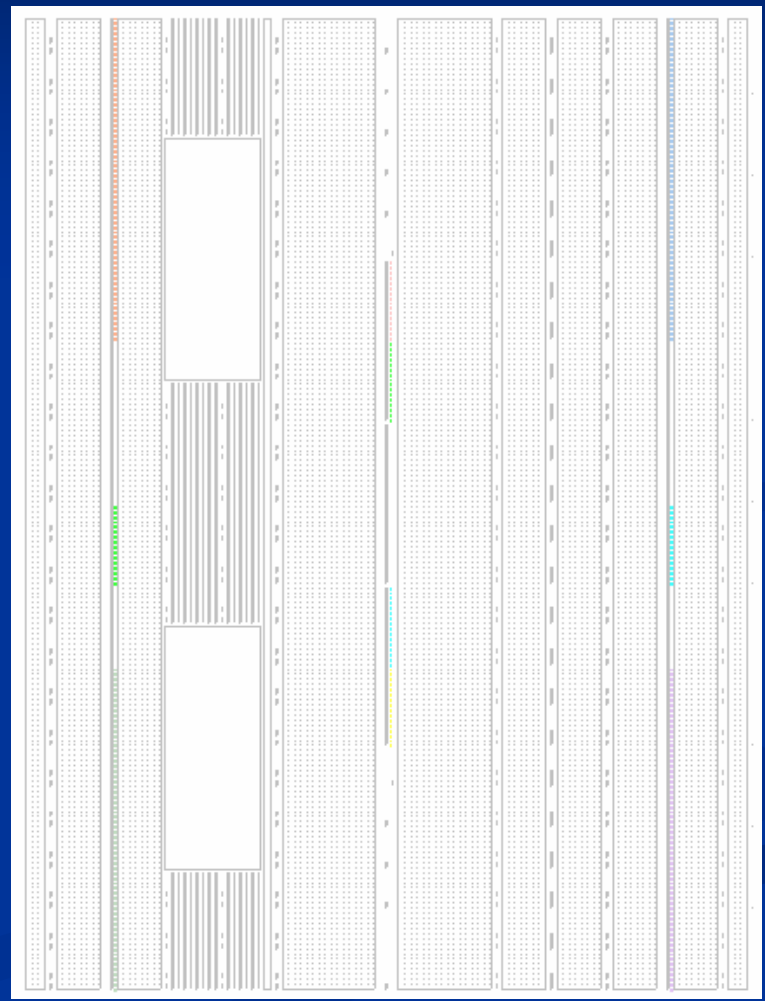
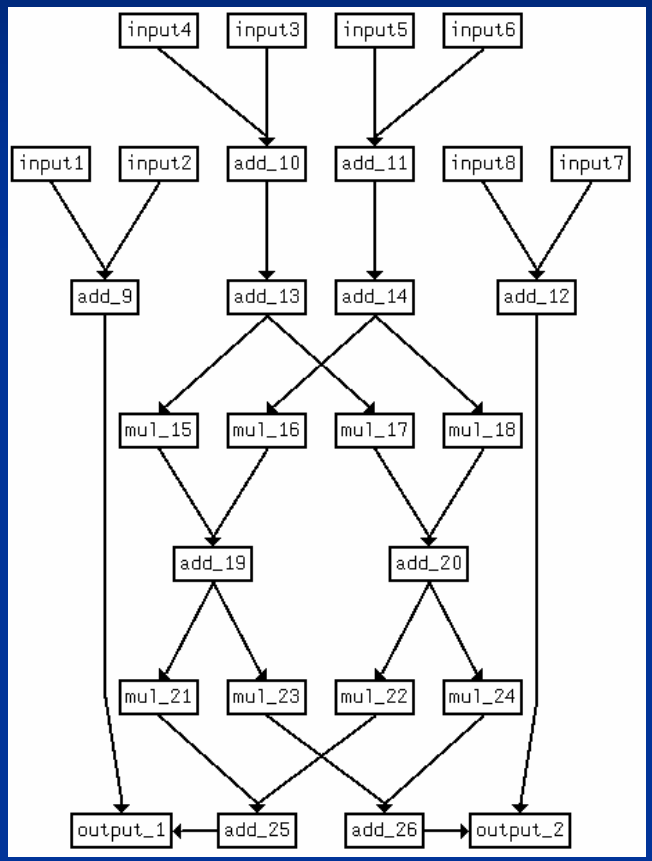
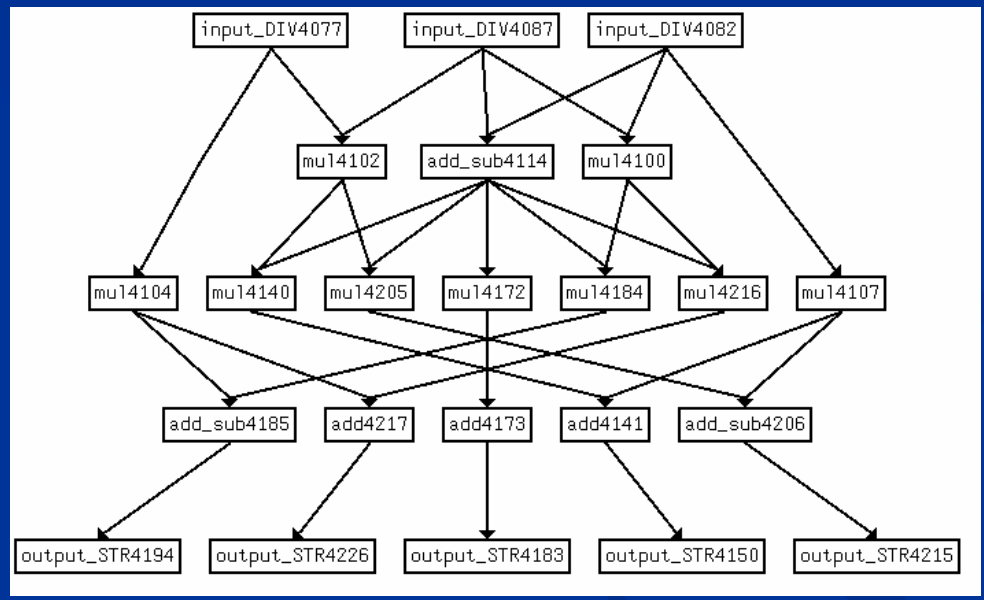


FPGA Virtex-4™ Board

Dataflow Graphs Overview

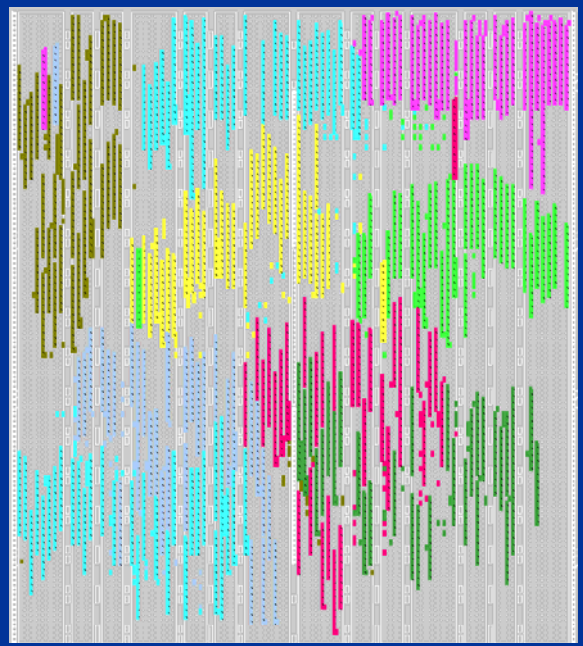


Design 1

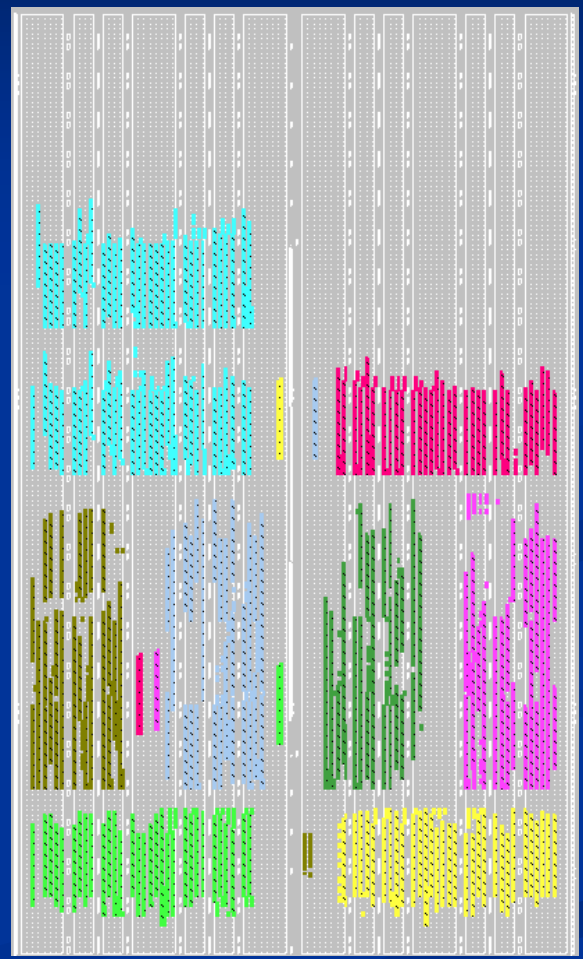


Design 2

Dataflow Graphs Considerations

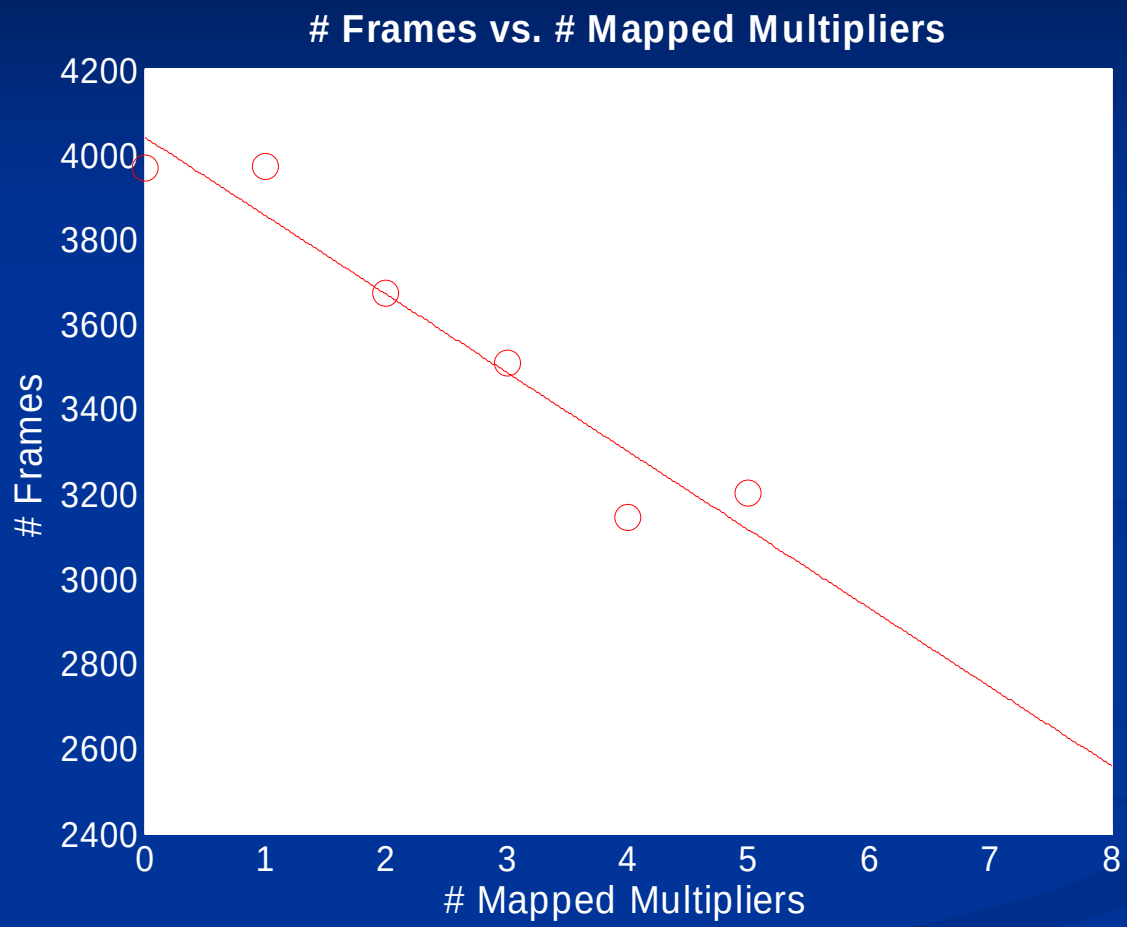


Unconstrained Design 2



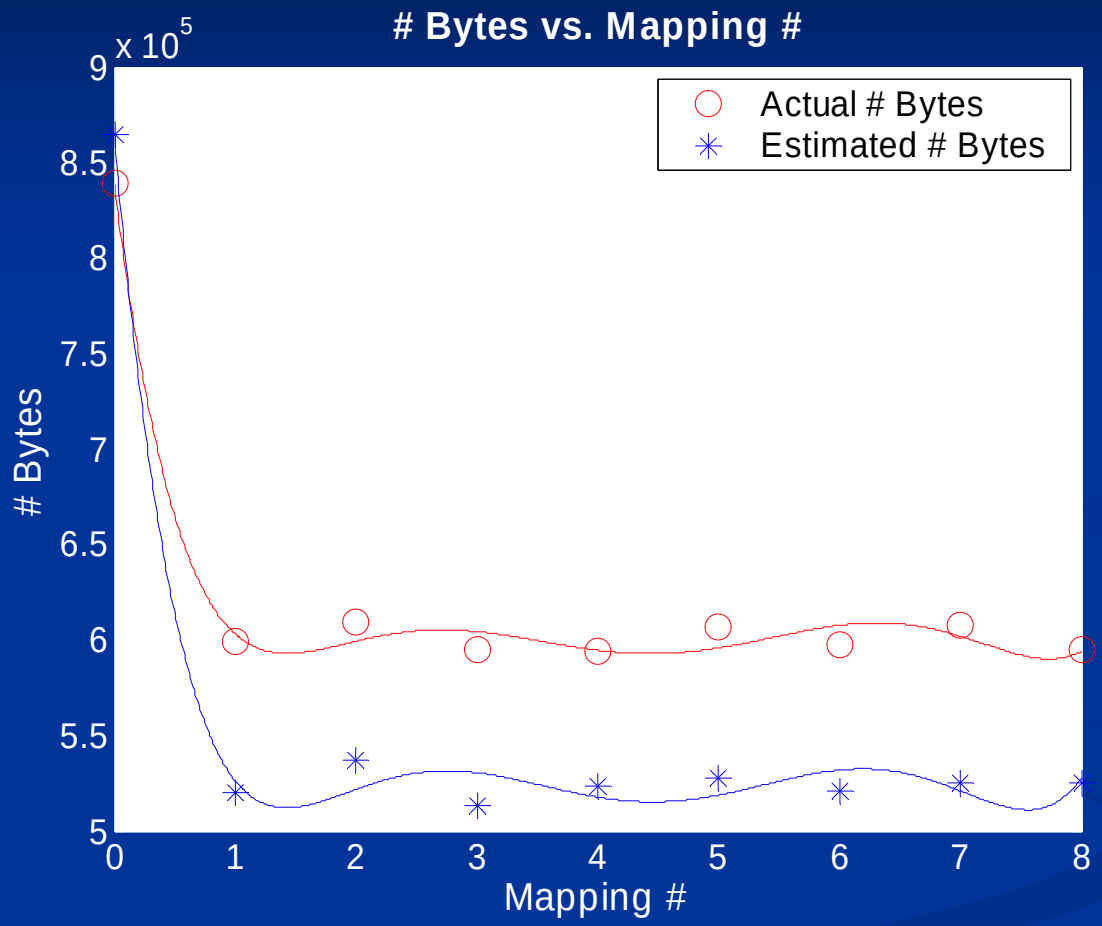
Constrained Design 2

Experiments – Unconstrained



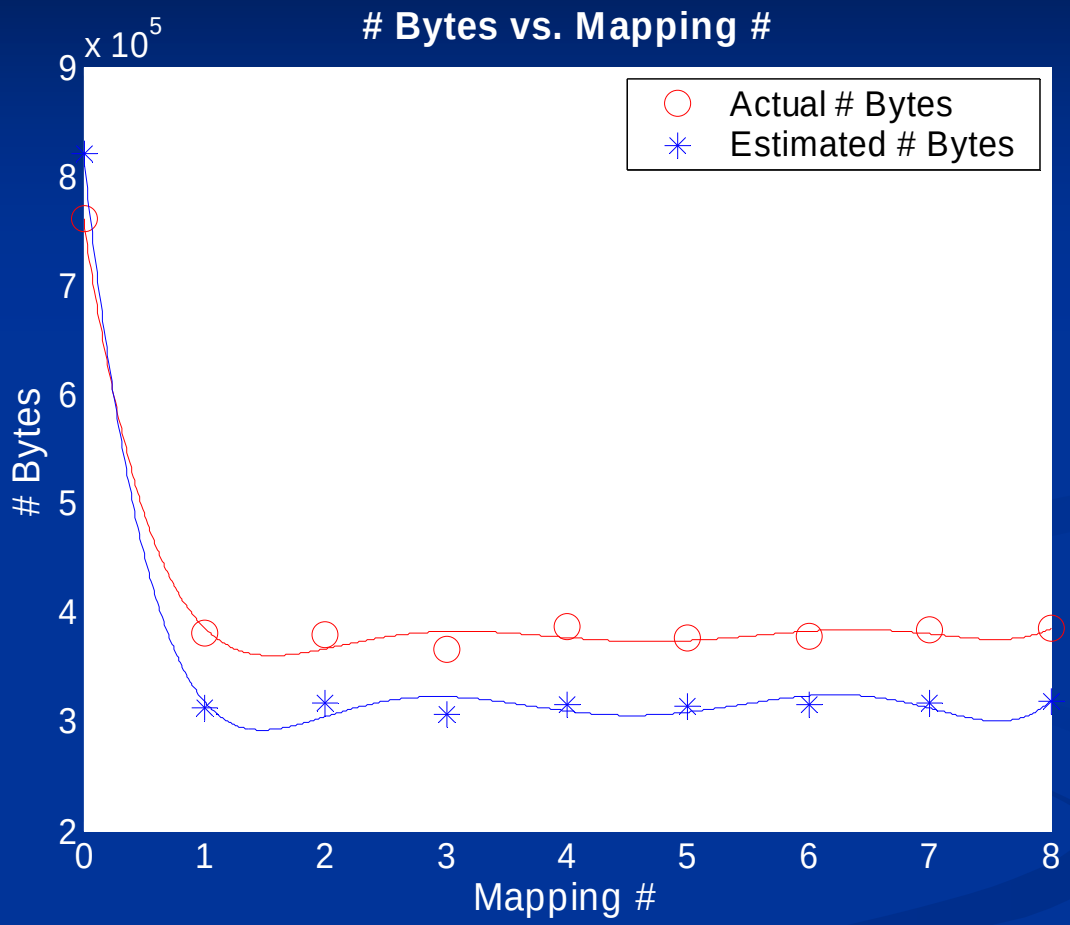
- Negative correlation between mapping and frames
- Design failed in Cases 6-8

Experiments – Constrained



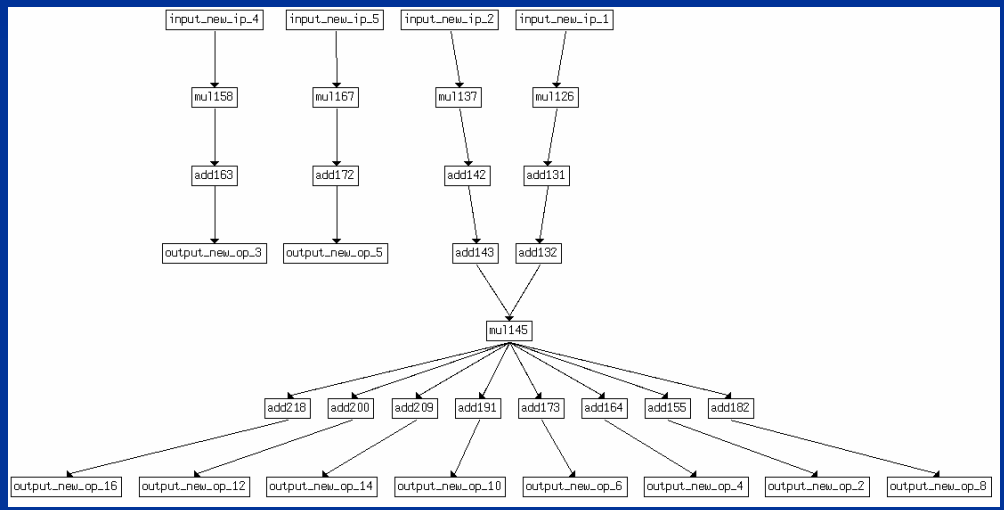
- Similar results for different mappings
- Substantial overhead for reconfiguration

Experiments – Interface

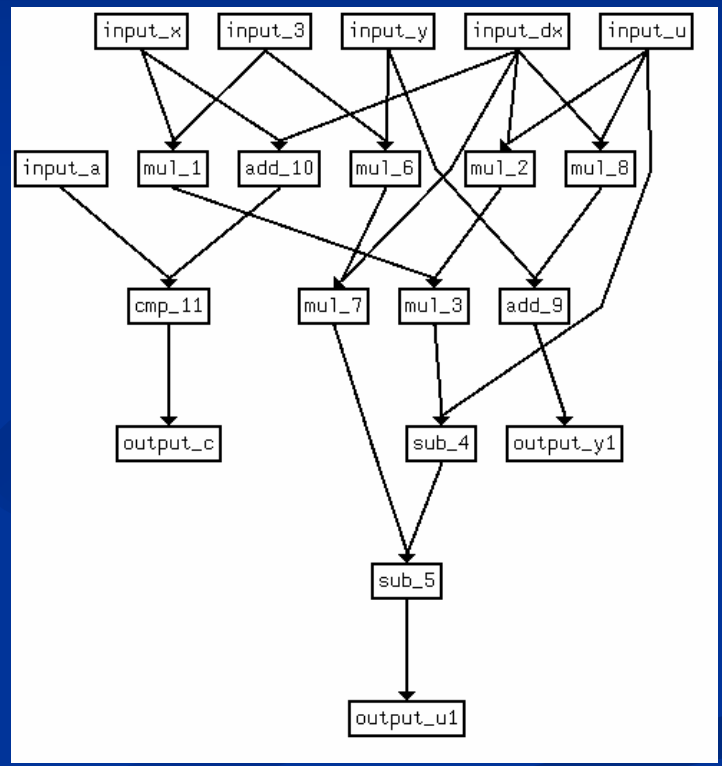


- Similar results for different mappings
- Fewer bits needed to reconfigure

Experiments – Mapping

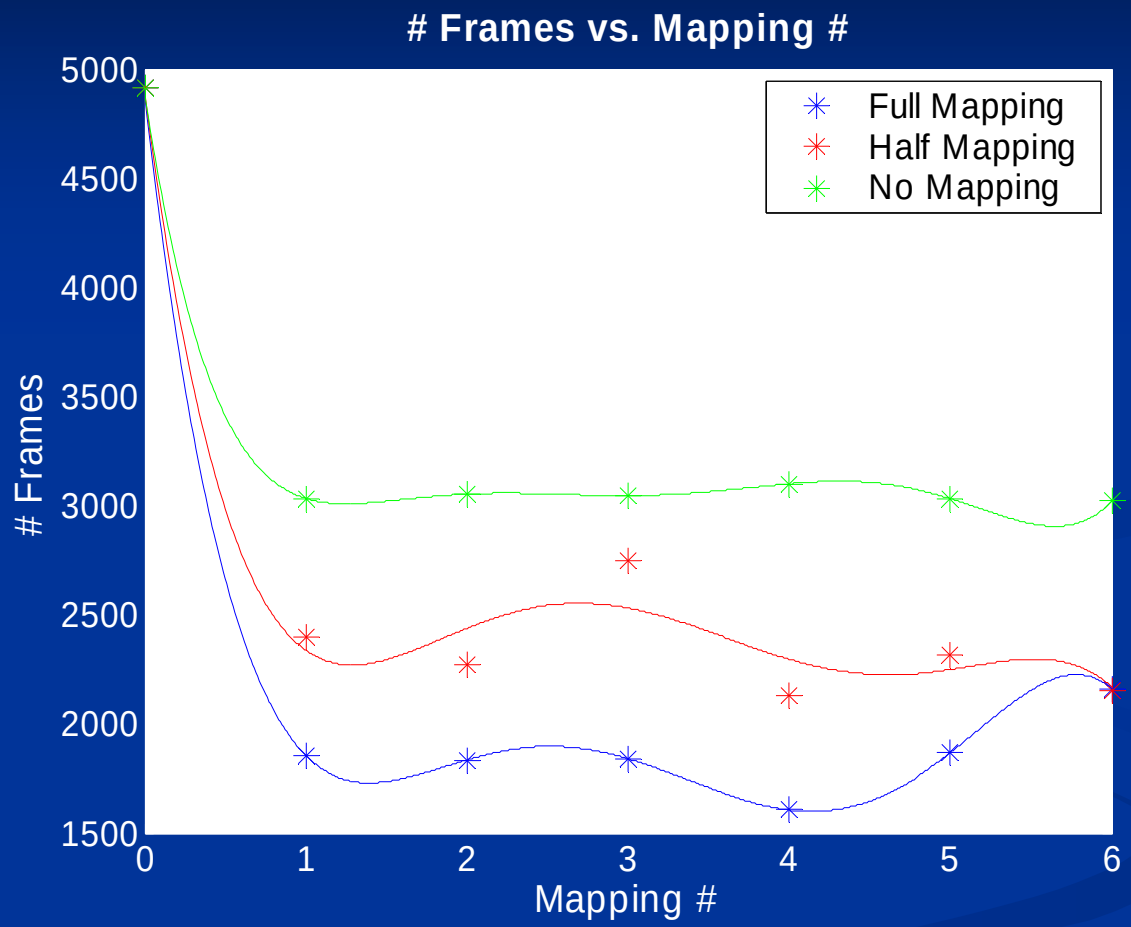


Design 3



Design 4

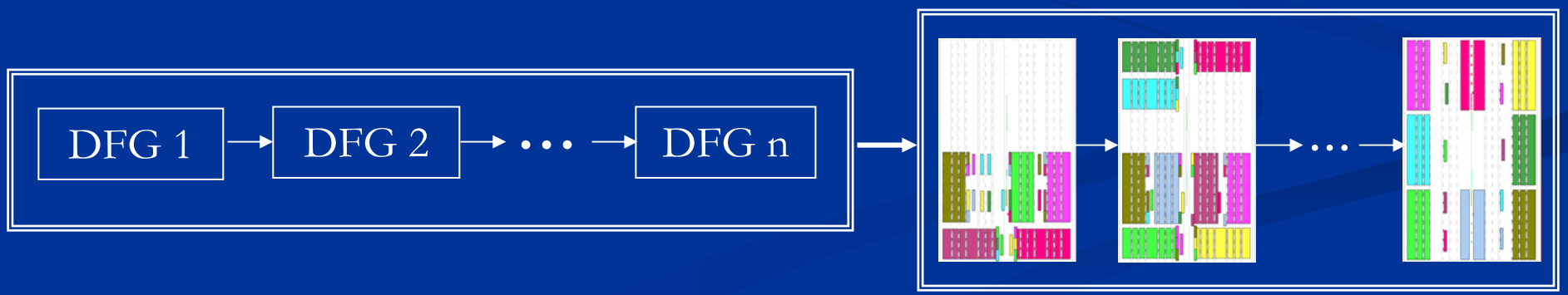
Experiments – Mapping



- The more mapping involved, the fewer frames needed
- More variation between different mappings

Future Work

- If placement failed, why?
  - Congested routing
  - Interface issues
  - Module Placement
- Systematic Layout



Conclusion

- Understand building blocks first
- Floor planning increases predictability
- Full mapping most beneficial, if possible
- Questions?